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# MODEL 168-D
# MICROPROCESSOR ANALYZER

# OPERATING AND SERVICE MANUAL

biomation

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OPERATING AND SERVICE MANUAL

MODEL 168-D

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# SECTION I

# GENERAL INFORMATION

## 1.1 Certification

Biomation Corporation certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

## 1.2 Warranty

All Biomation products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Biomation will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Biomation prepaid and Biomation will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF BIOMATION'S WARRANTY, BIOMATION SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL BIOMATION BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

## 1.3 Instrument Description

The Model 168-D Microprocessor Analyzer is a compact solid-state electronic instrument with specific features intended to aid the design engineer in the development of microprocessor-based systems. The unit allows direct real-time observation of software program execution within a system in the context of the hard-wired logic that surrounds a typical microprocessor.

A history of up to 256 memory accesses can be recorded, usually beginning with a Start event and terminating with a Stop event, via a personality/interface module that plugs into the system being monitored. The recorded information is displayed on a 9 inch CRT in one of four different display formats.

The Model 168-D is a bench-type instrument with a tilt-up stand and is fully self-contained with an integral CRT display and a comprehensive set of controls for data acquisition, manipulation, and display.

## 1.4 Specifications

SIGNAL INPUT

Load. Maximum current drain per line is 50 µA.

Connection: Via flat ribbon cable and unique Personality Module for each microprocessor type, 8 bit MPU only.

TIME BASE AND MEMORY

Clock Rate: Synchronous with system under development (SUD). Maximum 10 MHz.

Memory. 25 bits per word, 256 words.

ARM, START, STOP FUNCTIONS

Arm. Auto, External, Manual. Allows unit to search for Start event.

Start. Four hex character thumbwheel switch. Allows unit to begin recording system memory accesses.

Stop. Four hex character thumbwheel switch. Terminates recording.

Start/Stop Delay. Selectable delay for either event, up to 9999 memory accesses.

RECORD MODES

Normal. Unit records system memory accesses between Start and Stop events.

Halt. Unit records as in Normal mode, but stops system MPU when Stop event is detected. User may then single stop SUD manually, or select new stop event and resume recording.

DISPLAY

Memory. Data domain map of recorded memory accesses, displayed in a 16 X 16 data field. Most significant 8 bits of address word (Page) are displayed in hexadecimal characters.

Page. Data domain map of least significant 8 bits of address word (Address) is displayed in data field. Display is hexadecimal. Page on which these accesses occur is thumbwheel switch selected by user.

Sequential. Time domain map of recorded memory accesses. Single letter entry in data field for Read (R) and Write (W) accesses.

List. Detailed time domain map, in hexadecimal or binary, of memory accesses, 20 at a time. Cursor position determines which 20 accesses are displayed.

Cursor. Blinking underline, with vertical and horizontal positioning switches, used for readout of memory accesses. Position of cursor is fixed in memory between each display mode, when not recording.

EVENT OUTPUTS

Front panel BNC connectors provide Start, Stop, and Delayed Start/Stop outputs. A TTL level, positive going transition is output when respective events occur.

MISCELLANEOUS

Size.
HEIGHT: 10.25 in. (4 cm).
WIDTH: 21.25 in. (8.4 cm).
DEPTH: 15 in. (5.9 cm).
WEIGHT: Approximately 50 lbs. (22.7 Kg).

Power. Approximately 150 W, 115/230 VRMS, 50-60 Hz.

Warranty. All Biomation products are warranted against defects in materials and workmanship for one year from date of delivery.

Accessories. Each unit is supplied with a line cord, extender card, two copies of the Operating and Service Manual, and a choice of one Personality Module.

## SECTION II

## INSTALLATION

### 2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage, and installation of the Model 168-D.

### 2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Biomation representative or Biomation in Cupertino, California, U.S.A.

### 2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contact packaging companies in many cities can provide dependable custom packaging on short notice.

### 2.4 Power Connection

CAUTION: Before connecting the unit to AC power, be sure that the proper voltage has been selected.

The Model 168-D has a line voltage selector that permits operation at four different nominal line voltages: 100, 120, 220, and 240 VAC. The unit will operate correctly at variations of ± 10% from these nominal voltages.

The desired line voltage may be selected as follows:

1. Unplug line cord from rear of instrument.
2. Slide clear plastic cover to the left, and remove fuse using built-in lever.
3. Remove the small circuit board inside the fuse holder using a small hook or screwdriver.
4. Install the circuit board, oriented so that the desired line voltage is visible beneath the fuse clips.

5. Replace the fuse, slide the cover to the right, and replace the fuse. Use a 2-A slow blow fuse for all voltages.

Power cable: The Model 168-D is equipped with a detachable three-wire power cable. Proceed as follows for installation:

a) Connect line-cord plug (three-socket connector) to AC line jack at rear of instrument.

b) Connect plug (two-blade with round grounding pin) to three-wire (grounded) power outlet. Exposed portions of instrument are grounded through the round pin on the plug for safety. When only a two-blade outlet is available, use connector adapter, then connect short wire from side of adapter to ground.

## 2.5 Preparation for Use

The Model 168-D is an integrated, self-contained unit. Data may be captured and visually analyzed using the built-in CRT and operator controls. The following sections cover setup, operation, and interface requirements.

## 2.6 Initial Warm-Up

Although the Model 168-D is a solid-state instrument, a brief warm-up period of approximately 10 minutes is required for the internal circuitry to reach thermal stabilization.

# SECTION III

# PRINCIPLES OF OPERATION

## 3.1 Introduction

The advent of the microprocessor-based system has defined the need for a new type of analysis tool like the Model 168-D Microprocessor Analyzer. This unit provides specific features intended to aid the design engineer in the development of a microprocessor-based system. He can now observe software program execution within the system in real time, and in the context of the hard-wired logic that surrounds the typical microprocessor.

The unit records a history of up to 256 memory accesses, usually beginning with a Start event and ending with a Stop event. The recorded information is then presented to the operator in one of four different display formats. Two display formats present the data using memory maps, and the other two formats display the data as a function of time. By means of a cursor and control panel switches, the operator can examine selected data and transfer from one display format to another.

By use of a unique personality module for each type of microprocessor on the market, the user is able to get into his system with the Model 168-D. Two different operating modes and four different display modes enable the operator to acquire data from his system and then observe it from different points of view. The features contained in the Model 168-D provide a very powerful capability for troubleshooting the system software and hardware.

## 3.2 Description

The Model 168-D is interfaced to the system under development (SUD) via a personality module that is unique for a given microprocessor. The microprocessor chip in the system is unplugged from the system and plugged into the personality module as shown in Figure 3.1. The module interface plug is then plugged into the microprocessor socket in the SUD. This action allows the 168-D to monitor memory access information within the SUD. A memory access is defined as the operation the SUD microprocessor goes through to read out of, or write into, the memory of the SUD.

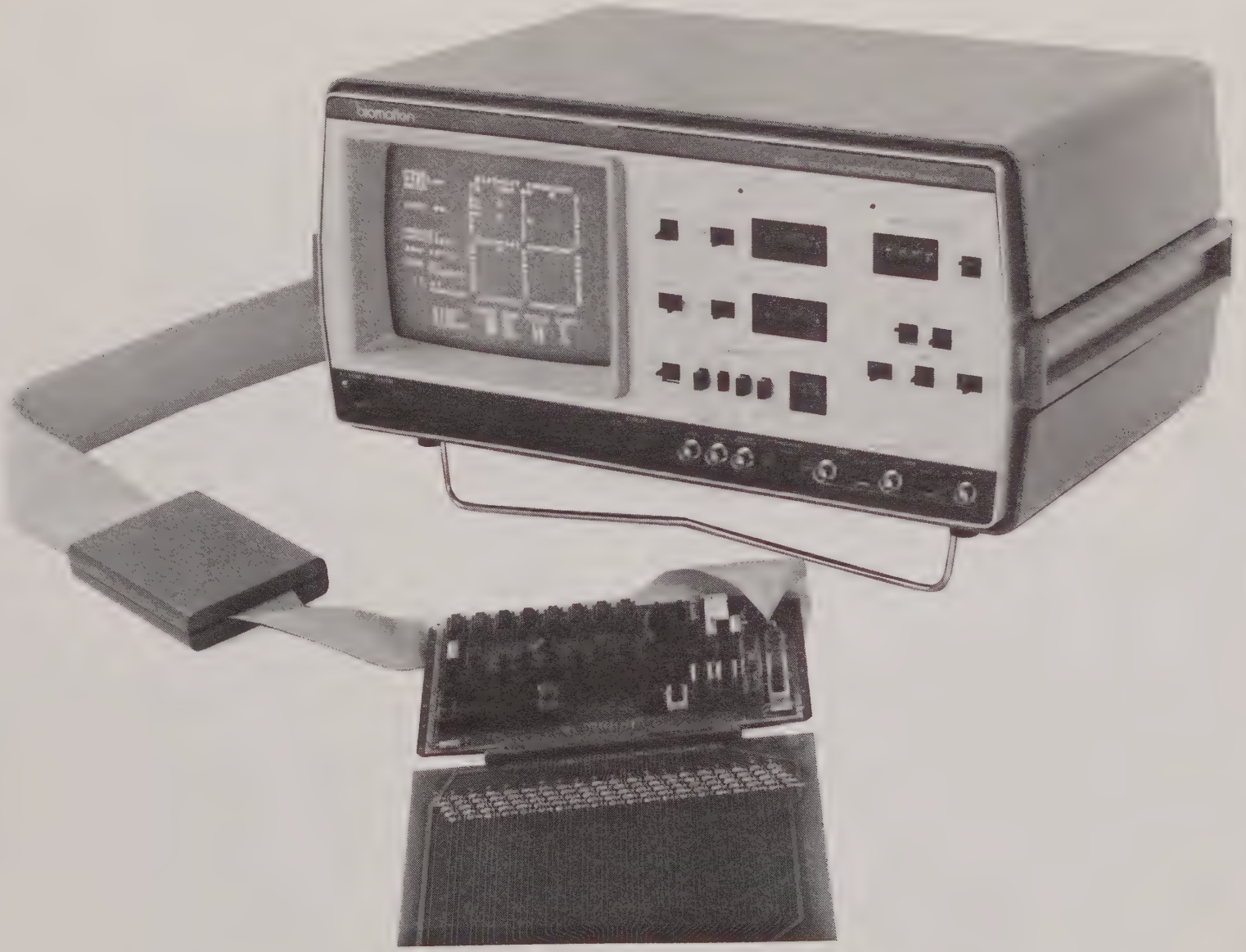


Figure 3.1 Model 168-D with personality module.

The 168-D has a memory with a 256 word capacity. Each word is 25 bits wide. This provides for 16 bits of address information, 8 bits of data, and 1 bit that signifies either a Write or Read operation. The contents of the memory in the 168-D may be examined via the built-in 9-in. CRT monitor.

Once the 168-D has completed a record sweep, the operator may select any one of four different display modes with which to view the data. The data is presented in alphanumeric form. The data associated with the memory accesses of the SUD is presented in hexadecimal form in three of the display modes. The fourth display mode provides, by switch selection, a 24-bit 1-0 pattern in a listing format or in a hexadecimal listing.

## 3.3 Recording

The 168-D uses the clock from the SUD to record the results of a memory access by the SUD microprocessor. The internal workings of the microprocessor are not recorded. The software instructions defining the SUD tell the microprocessor to read from or write into the SUD memory. Whenever the microprocessor accesses (reads out of or writes into) its memory, the transaction, or access, is recorded into the memory of the 168-D. These accesses can be recorded at rates up to 10 MHz. The 168-D records the address (16 bits) of the access, the data stored at that address (8 bits), and whether the operation was a read or write operation (1 bit). The 168-D can record 256 such addresses for any given record sweep.

## 3.4 Record Control

The Model 168-D is designed to be a transparent instrument; i.e., the unit passively records the data available without interruption of, or influence on, the SUD. It does this in real time, or at the rate at which the data is actually being transferred within the SUD. This is known as the Normal record mode.

In the Halt mode, the instrument will passively record, and allow the SUD to function normally. At a preselected point, the 168-D will halt the operation of the microprocessor in the SUD. The Halt record mode allows the user to use the single step capability of the instrument.

The single step operation is useful when the user has a program that functions correctly to a certain point. After this point, the program enters an undefined state, or perhaps goes into a defined state that is not allowed, given the preceding conditions. The user can start recording at a known point in the program, and stop recording just prior to entering the unknown state. At this point, the 168-D can be preset to halt the operation of the SUD microprocessor. The user may then single step the microprocessor and record memory accesses. In this fashion, the steps leading to an undefined or prohibited state may be captured and analyzed.

Convenient front panel controls allow the user to define the recording options to be used for a particular record sweep. The Start event controls allow the user to define, using a four hex character word (16 bits), the beginning of the record cycle. This Start event word can be further qualified to be a Read, a Write, or either operation. The source of the Start event may be selected to originate from an external event or an internal event.

A four hex character word may also be selected for the Stop event. Read, Write, or either access is also available as a qualifier. In addition to the external or internal source of the Stop event, this event can also be selected to be the End of Storage (stop when memory full).

Either the Start or Stop event may be delayed by using the delay thumbwheel. The influence of these events on the instrument is thus delayed. The Stop event may be considered a post trigger, allowing capture of prior trigger information. The Start event may be considered a qualifier to begin recording. The Start and Stop events may be so positioned, with respect to the SUD program, that less than the entire memory of the 168-D will contain SUD memory accesses.

The operator has complete control over the acquisition of data from the SUD. He can select the Normal operation, which allows the 168-D to collect the data defined between the Start and Stop events. The SUD microprocessor free runs. If the user selects the Halt record mode, the microprocessor in the SUD will be halted on the occurrence of the (delayed) Stop event. The user can then use the Single Step switch to step the SUD microprocessor.

The instrument has been designed so that it can acquire data from any microprocessor system operating at memory access rates to 10 MHz. Thus, the instrument can be used on all present microprocessor systems and will be able to keep pace with developments in memory access speeds.

The operator can cause the 168-D to record microprocessor memory accesses, Direct Memory Accesses (DMA), or both, by means of a switch on the control panel. This permits him to observe the activity between the SUD memory and the microprocessor, a CRT or floppy disc (DMA), or both microprocessor and DMA device, provided the 168-D has direct access to the SUD bus.

## 3.5 Display Output

The Model 168-D has a built-in 9-in. raster scan CRT. The unit has very versatile display controls so that the user can select the display mode that displays the information in the most efficient manner for a given approach to debugging the program or hardware.

The memory capacity of the 168-D is 256 words, 25 bits per word. Each word is composed of the following: 16 bits made up of the SUD address, broken into Page (8 MSBs) and Address (8 LSBs); 8 bits of data; one bit to signify Read or Write access.

There are four distinct display modes available in the Model 168-D. The Memory display mode presents the "big picture" of memory activity to the user. The data array contains four groups of 64 characters each. This total array represents all the memory "pages" within the Model 168-D, namely 256. The characters displayed within the data array represent the "page" numbers (8 most significant bits of the 16 bit address word) that were accessed by the SUD microprocessor during the record sweep of the Model 168-D. One or more accesses on a page is signified by an asterisk on the CRT in the position associated with that page. By comparing the page numbers displayed in this mode with a listing of the user's program, he can determine if his system has occupied any undefined or disallowed states.

When the Page display mode is selected, the 168-D will display all access activity on a selected page from its memory. The user selects the desired page using the two hexadecimal thumbwheel switches provided. In this mode, the data array is made up of the 8 least significant bits of the 16-bit address word. Displayed in the array area are Rs and Ws indicating Read and Write operations. An X in the data array signifies that both a Read and a Write operation has occurred at this address location.

The Page mode allows the user to begin looking more minutely at the information that is being generated by the SUD.

In the Sequential display mode, the data array presents a sequence of the accesses as they were recorded in the memory of the 168-D. The first access recorded in memory is presented in the upper left hand corner, the second access immediately to the right of it, and subsequent accesses displayed as one would read a page of printed information. A maximum of 256 accesses can be displayed in this mode, which would indicate that the entire memory of the 168-D has been filled with memory accesses from the SUD. The Start and Stop event words may be chosen such that the memory of the 168-D contains less than 256 accesses. The Sequential display mode allows the user to trace the execution of the program between the Start and Stop events.

In the Memory, Page, and Sequential display modes, the Start and Stop events are displayed in the lower portion of the CRT. In the Memory and Page modes, the Start and Stop events, if displayed in the data array, are blinked for identification.

The List display mode allows the user to view the memory contents of the 168-D in a sequential mode, but this time the data is presented a line at a time. The earliest access is placed at the top of the screen, and the latest access is placed at the bottom. Twenty memory accesses are displayed at a time. The data displayed on the screen may be "scrolled," so that the entire memory of the 168-D may be viewed through a 20 access window.

The data is presented in hexadecimal code, plus an R or W for Read or Write accesses. If desired, the user can select a binary display. The information in memory is then presented line by line, each line six groups of four bits each, with a 1/0 column for Read/Write indication.

The List mode allows direct comparison of the accesses recorded in the 168-D memory with the user's program listing. The List mode displays the data accessed by the SUD as a function of time.

## 3.6 Display Cursor

The versatile cursor is included in the display output to allow the reading of information and to keep track of the point in the SUD program at which the user is examining the SUD (among the four display modes). The cursor position is consistent. If a word is selected in one display mode, the user may go to another display mode and the cursor will remain with that word selected. The exception is that if a word is selected in the List or Sequential modes, and the user goes to the Page mode and selects a page on which the word is not located, the cursor will relocate itself to the "home" position in the center of the data array. If the word is present on the page selected, the cursor will go to that particular word.

In the Memory, Page, and Sequential display modes, the cursor enables the user to read address and data information. The cursor is positioned at a particular access. The address and data information are displayed in the lower portion of the CRT.

A pair of spring loaded switches are provided to move the cursor about in the data array. The cursor vertical movement switch also controls the scrolling of the data in the List mode.

## 3.7 Inputs and Outputs

Six front panel BNC connectors allow input and output of various signals. The input connectors allow the user to input an Arm signal, a Start signal, and a Stop signal. The user can select positive or negative slope sensitivity for the Start and

Stop input signals. The input threshold for these three inputs is selectable via a switch. Preset TTL levels for X1 and X10 probes are available, as well as a variable position to allow for thresholds between $\pm$2 V. The variable adjustment is inside the unit. The Arm, Start, and Stop signal inputs provide the same control of the unit as do the internal Arm, Start, and Stop events.

In addition, the event output BNCs provide Start, Stop, and delayed Start/Stop events. The Start event output occurs as soon as the Model 168-D detects the Start event selected by the four thumbwheel switches.

The Stop event output occurs when the Model 168-D detects the preselected Stop event.

The delayed Start/Stop event occurs when the preselected delay, with respect to the Start or Stop event, is counted out.

# SECTION IV

# OPERATION

## 4.1 Introduction

This section identifies and describes front panel controls, displays, and personality modules of the 168-D Microprocessor Analyzer. A thorough understanding of this section is essential for successful use of the instrument. Before starting, refer to Figure 4.1.

## 4.2 Control Panel Indicators. Refer to Figure 4.1.

### 4.2.1 Search

4.2.1.1 START EVENT (1) - This yellow LED, when on, indicates that the unit has been armed and is searching for a Start event.

4.2.1.2 STOP EVENT (2) - This yellow LED, when on, indicates that the unit has recognized a valid Start event and is searching for a Stop event. The unit is recording when this LED is illuminated.

4.2.2 RECORD (3) - This yellow LED, when on, informs the operator that the unit is presently recording information. In the NORMAL record mode, this indicator will go off when a Stop event is recognized. In the HALT mode, the indicator will remain lit in recognition of a Stop event, indicating that the microprocessor has been halted but information may still be recorded when the Single Step switch is activated.

4.2.3 BUFFER FULL (4) - This yellow LED, when on, indicates that the 256 word storage area of the unit has been filled to capacity with memory accesses.

## 4.3 Delayed Start/Stop Event

4.3.1 MEMORY CYCLES (5) - This four wide, 16 position switch array is used by the operator to preset the number of memory cycles to be delayed before recording begins, or the number of memory cycles to be counted before recording terminates, depending on the setting of the Start-Stop switch (6). Delay can be preset up to 9,999 memory cycles.

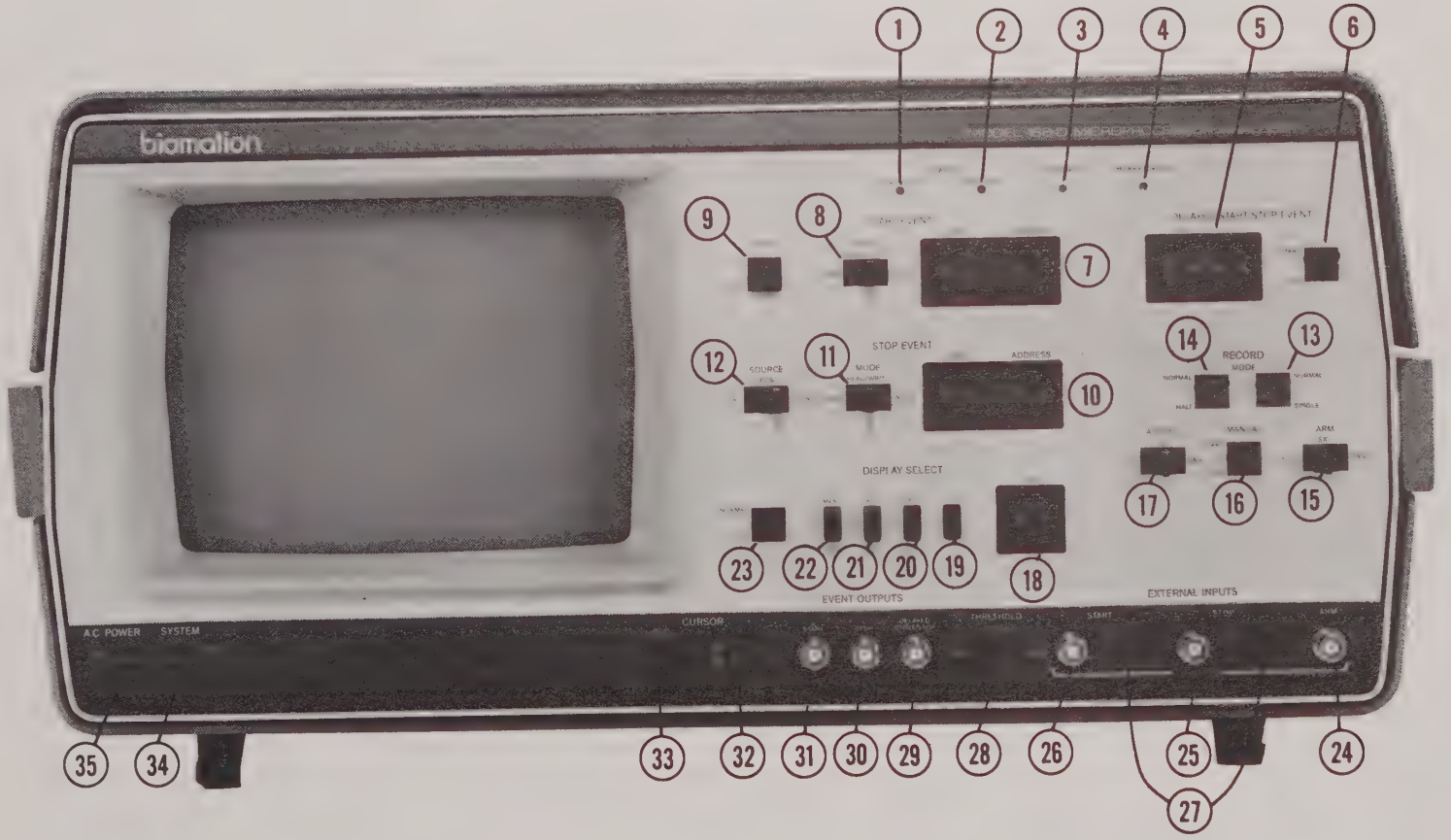



Figure 4.1 Front panel functions.

4.3.2 START-STOP Switch (6) - This switch, when in the START position, will cause the unit, after recognition of a valid Start event, to count the preset number of memory cycles before commencing recording (Figure 4.2a). In the STOP position, the unit will recognize a valid Stop event, and then count the number of memory cycles before recording terminates (Figure 4.2b).

## 4.4 Start Event

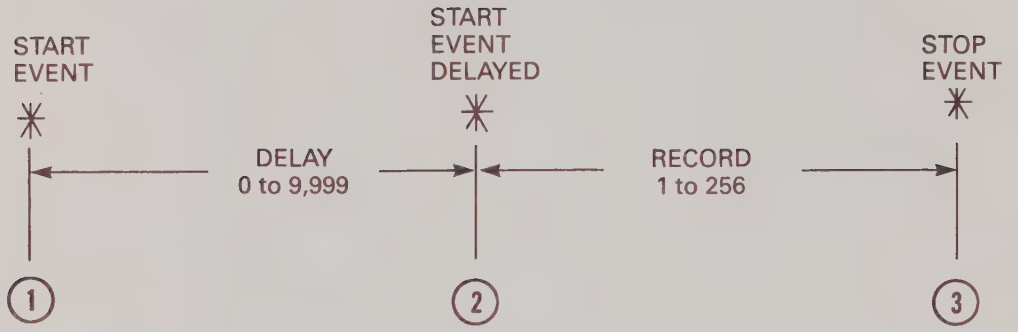
4.4.1 PAGE-ADDRESS (7) - This four wide, 16 position switch array allows the operator to preset the Page (upper 8 bits of address) and Address (lower 8 bits of address) that the unit should recognize and commence recording or counting the preset delay before recording. Switch coding is hexadecimal.

4.4.2 MODE (8) - This three position switch allows the operator to further qualify the Start event. In the READ position, the unit will recognize only an access on the preset Page and Address that was a read operation. In the WRITE position, the unit will recognize only an access on the preset Page and Address that was a write operation. In the READ/WRITE position, the unit will commence recording delay on any operation that occurs on the preset Page and Address.

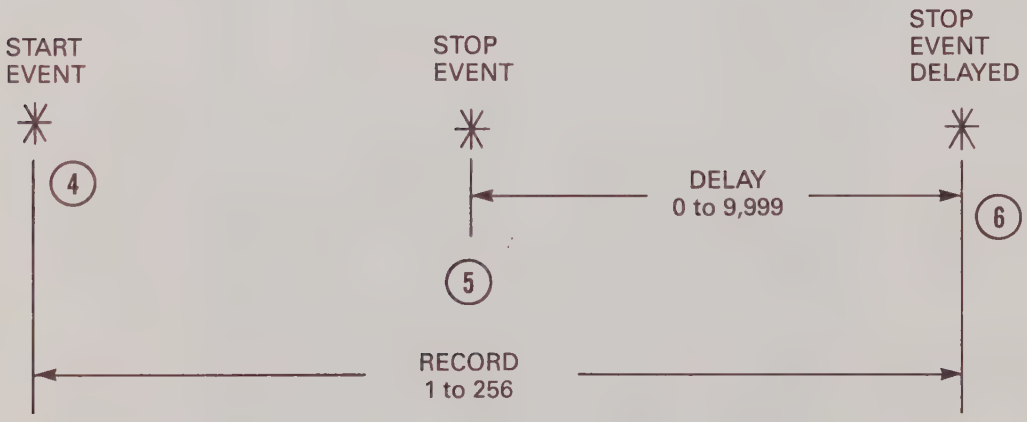
4.4.3 SOURCE (9) - This two position switch allows for the selection of the Start event source. In the EVENT position, the unit will search for the Start event qualified by the Page, Address, and Mode switch positions. In the EXT position, the Page, Address, and Mode settings will be disregarded and the unit will commence recording or counting delay only upon receipt of an external Start event signal.

## 4.5 Stop Event

4.5.1 PAGE-ADDRESS (10) -This four wide, 16 position hex coded switch array allows the operator to preset the Page (upper 8 bits of address) and Address (lower 8 bits of address) that the unit should recognize and terminate recording, or begin counting the preset delay, before ending a record cycle.




DELAYED/START EVENT a.




DELAYED/STOP EVENT b.

Figure 4.2 Controlling events for recording.

4.5.2 MODE (11) - This three position switch allows the operator to further qualify the Stop event. In the READ position, the unit will recognize only an access on the preset Page and Address that was a read operation. In the WRITE position, the unit will recognize only an access on the preset Page and Address that was a write operation. In the READ/WRITE position, the unit will terminate recording, or begin counting delay, on any operation that occurs on the preset Page and Address.

4.5.3 SOURCE (12) - This three position switch allows for the selection of the Stop event source. In the EVENT position, the unit will search for the Stop event qualified by the PAGE, ADDRESS, and MODE switches. In the EXT position, the Page, Address, and Mode settings will be disregarded and the unit will terminate recording, or counting delay, only upon receipt of an external Stop event signal. In the EOS position, the unit will terminate recording, or begin counting delay, when the 256 word storage area has been filled, provided the Stop event qualified by PAGE, ADDRESS, and MODE switches did not occur before the buffer was filled. In this switch setting, the unit will recognize either the Stop event or the EOS (end of storage), whichever occurs first.

## 4.6 Record

4.6.1 MODE (13) (14) - These two switches allow the operator to control recording of memory accesses of the microprocessor. With both switches in the NORMAL position, the unit will record transparently. With switch 14 in the HALT position, the unit will allow transparent recording down to the specified Stop event conditions and then halt the microprocessor. The SINGLE STEP switch (13) can then be used to single step the microprocessor. A single depression of the switch causes the microprocessor to execute one instruction cycle. A repeat function is also provided, whereby, if the switch is held down, one access is permitted. After a 500 msec pause, accesses are allowed to occur at the rate of one every 200 msec.

4.6.2 ARM (15) - This switch controls the arming of the unit. In the AUTO position, the unit will arm itself and search for a Start event. After recording, the unit will display the record and rearm itself for a new record. In the EXT position, the unit can be armed by injection of the proper signal on the ARM input BNC. The unit may also be armed by momentarily switching the Arm switch to the MANUAL position. The switch is spring loaded to return to the EXT position. In all modes of arming, the SEARCH-START EVENT LED will illuminate, indicating unit readiness for Start event recognition.

4.6.3 MANUAL (16) - This switch allows the operator to manually commence or terminate recording. The unit, however, must be armed before a manual start can be initiated.

4.6.4 ACCESS (17) - This three position switch allows for the selection of types of memory accesses that are to be recorded. In the DMA position, the unit will record only those accesses that are direct memory accesses, or those accesses not made by the system microprocessor. In the µP position, the unit will record only microprocessor memory accesses. In the ALL position, the unit records both DMA and microprocessor accesses.

For those MPUs that require buffering of output signals (fan-out of one), the 168-D cannot monitor system bus activity. Thus, only microprocessor memory accesses may be recorded because the 168-D is isolated from the bus by the buffers.

## 4.7 Display Select

4.7.1 PAGE (18) - This two position, hex coded switch array is used by the operator to select the specific page for viewing.

4.7.2 LIST (19) - Allows selection of the List display.

4.7.3 SEQ (20) - Allows selection of the Sequential display.

4.7.4 PAGE (21) - Allows selection of the Page display.

4.7.5 MEM (22) - Allows selection of the Memory display.

4.7.6 NORMAL/SELECT (23) - This three position switch provides normal display modes when in the normal position. Depression provides the selection of alternate display functions that are determined by the display selected. Center position is Select standby. Lower spring loaded position enables Select functions, which are explained below in Section 4.13.

## 4.8 External Inputs

4.8.1 ARM (24) - An external connection point (BNC) allows the unit to be armed by injection of a 1.5 µsec positive pulse that exceeds the preset threshold. The ARM switch (15) must be in the EXT position. Input is clamped to $\pm$ 5 V.

4.8.2 START, STOP (25), (26) - These BNC connectors allow the injection of pulses that will commence and/or terminate the record process when the SOURCE switches (9 and 12) are in the EXT position. The pulse width must be at least 1.5 µsec and exceed the preset threshold level. Switches are provided (27) for slope selection of the triggering signal. Inputs are clamped to $\pm$5 V.

4.8.3 THRESHOLD (28) - This switch selects the threshold levels for the Arm Start and Stop external inputs. The levels are TTL X1 (+1.4 V) for X1 scope probes, TTL X10 (0.14 V) for X10 scope probes, and Variable, which is set by a potentiometer inside the unit. The adjustment is on the right upper corner of the front panel PC board (when viewed from the front). The top cover of the unit must be removed to gain access. The pot is labeled THRESHOLD ADJUST. A test point is available just below the pot to allow measurement of the threshold. Adjustment range is ±2.5 V.

## 4.9 Event Outputs

4.9.1 START, STOP (30), (31) - Provides a 50 nsec positive going TTL pulse when a valid Start event and a valid Stop event is recognized.

4.9.2 DELAYED START/STOP (29) - Provides a 50 nsec positive going TTL pulse when the preset delay (5), defined from a Start or Stop event (6), is counted down.

## 4.10 Cursor (32), (33)

These switches provide horizontal and vertical control of the cursor in the displays.

## 4.11 System Clear (34)

This switch, when raised, clears the memory of the unit. It also resets the cursor to memory location 1. If switch (34) is not used, the cursor will remain at a selected 168-D memory location from one record sequence to the next.

## 4.12 Power ON/OFF (35)

A red LED is provided to indicate when power is applied to the unit.

## 4.13 Display Modes

To describe adequately the different display modes, sample recordings have been taken. These recordings and the resultant displays are for illustrative purposes only.

### 4.13.1 Memory Mode

Figure 4.3 illustrates the Memory display mode. This is the "big picture" of system activity, from a data domain standpoint. We can see that the system accessed pages Ø3 and ØC. A page here is defined as the most significant 8 bits of the 16 bit microprocessor address word. These bits are mapped in the data field of the CRT, which are the four blocks in the display, each an 8 x 8 matrix.

Under MEMORY ACCESSES: there were 256 accesses (256 TOTAL) recorded (the memory of the 168-D is full), and the cursor (blinking underline) is positioned at analyzer memory location 239 (239 TO CURSOR). The notation 215 AT CURSOR indicates that the analyzer recorded 215 accesses on page ØC.

At the bottom of the display, the Start and Stop events are shown, along with the recorded information at the cursor position. Asterisks will appear immediately to the left of the words START and/or STOP if the first and/or last access in the 168-D buffer was the same page, address, and operation as defined by the Start and Stop events that were preset on the front panel prior to recording. The cursor position readout (CURSOR, at display bottom) shows the LAST access in time on Page ØC that is in the analyzer's memory. The hexadecimal representation is ØC Ø7 Ø8.

To read the information at all 215 accesses on page ØC, the user presses the NORMAL/SELECT switch (23) once for every step. This decrements the cursor position. Figure 4.4 shows the next earliest access (214 AT CURSOR) obtained by pressing the Select switch. The hex data at this access is ØC Ø6 ØØ.

The cursor sorts through the memory of the 168-D, retrieving accesses that are on the same page. This relieves the user from the tedium of looking through all 256 accesses to pick out visually all accesses on a given page.

### 4.13.2 Page Mode

The cursor position is fixed in the analyzer's memory when switching from one display mode to the next. In the Memory and Page modes, the NORMAL/SELECT switch (23) must be in the center position. If in NORMAL position, the cursor will automatically locate the latest selected access.

Figure 4.5 illustrates this property. We have selected the Page display mode. Note that TO CURSOR is still 237, which means that we are looking at the same access, with the cursor, as in Figure 4.4. Now, instead of the "big picture," we are taking a more detailed data domain look at the recorded data.

In the Page mode, the data field maps the least significant 8 bits of the 16 bit word (here referred to as the address). The user selects a particular page he wishes to view, and all addresses (8 LSBs) associated with that page are mapped. The display shows PAGE ØC selected. The cursor is at address Ø6. AT CURSOR tells us that 24 accesses occurred at ØC Ø6. The cursor displays the data at the 24th access. If the user wishes to view the data at each access, he decrements the cursor as in the Memory display mode. Now, the cursor sorts both page and address.

### 4.13.3 Sequential Mode

Without changing the cursor position, we select the Sequential display mode. In Figure 4.6, we can see that the entire memory of the 168-D is full. Each of the 256 data field locations represents a memory location in the 168-D. These are arranged in time as one would read a page of printed matter. The earliest access is at the upper left, and the latest is at the lower right. The Sequential display mode gives the user a time domain macro picture. Note that both Read (R) and Write (W) accesses occurred during this record sweep. The normal Sequential display will show only Rs and/or Ws. Figure 4.6 shows S entries also. An S will appear at every location that has the same 16 bit address as the cursor word when the NORMAL/SELECT switch (23) is depressed. The cursor occupies the same position in memory as it did in Figure 4.5 (237 TO CURSOR).

### 4.13.4 List Mode

The List display mode allows the user to minutely examine the data in the time domain. Figure 4.7 shows 20 memory accesses at a time, earliest at the top, latest at the bottom. The cursor is in the same memory position as before and is displayed at the center of the list. The cursor position determines which 20 accesses are displayed at any one time. The total number of memory accesses stored in the 168-D is displayed by MEMORY ACCESSES. The number by TO CURSOR shows the cursor position within the 168-D's storage area.

All data displays up to this point have been in hexadecimal code, the common programming code of microprocessor systems. If the user wishes to view his data in binary format, he may do so in the List mode by pressing down the NORMAL/SELECT switch (23). The data in Figure 4.8 shows the data from Figure 4.7 in binary code.

## 4.14 6800 Personality Module Controls

In the 6800 personality module (Figure 4.10) there is an 8 wide DIP switch. The position of these switches determine whether or not an upper address line (page information) is observed and recorded by the 168-D. This allows the operator to switch out memory pages which do not exist in his system. The lines will then appear as zeros to the 168-D and be recorded as such. There are also two connection hooks marked DMAR (Direct Memory Access Request) and DMAC (Direct Memory Access Clock). These allow the user to record direct memory accessing of his system by proper connection to points within his system.

## 4.15 8080A Personality Module Controls

In the 8080A personality module (Figure 4.9) there is a 10 wide DIP switch. The first eight positions function as do the switches in the 6800 personality module. Switch 9, when on, allows the user to record status information that is presented by the 8080 on the data bus immediately following a memory access. This will, however, cut in half the number of memory accesses that can be recorded (128 as opposed to 256) but does provide additional information in the form of microprocessor status. In the OFF position, status bytes will not be recorded, only memory accesses. Switch 10 has no function. The DMAR AND DMAC connective points have the same function as those in the 6800 personality module.

## 4.16 Counting Loop Iterations

Loop iterations are counted using a counter set up to count events. The counter is connected to the Stop Event output on the front panel of the 168-D. Each time the 168-D encounters the selected Stop Event, the counter gets incremented by the Stop Event output pulse. The 168-D is operated in the Halt record mode in order not to miss a Stop event during its display mode.

Set the 168-D controls as follows:

Start Source: Event
Mode: As desired
Page/Address: Any address upstream of the loop to be counted; can be entry statement.
Delay: 0000

Stop Source: Event
Mode: As desired
Page/Address: Any desired address in the loop to be counted.
Delay: 0000
Record Mode Normal/Halt: Halt
Normal/Single: Normal

Access: µP
Arm: Auto
Display Select: List

Set the counter to count events. Connect the Stop Event Output BNC to the event count input of the counter.

Clear counter and 168-D. Open counter gate, and then reset SUD.

Note that, because the Halt Record Mode is being used to make this measurement, the SUD WILL NOT be operating at real time rates. The counter will display the number of times the SUD executed the loop.

At the end of the count, all four amber LEDs will be on. To ready the 168-D for the next measurement, select ARM EXT, NORMAL RECORD MODE, CLEAR, and ARM MANUAL, in that order.

## 4.17 Measuring Loop Execution Time

Loop time is measured by a frequency counter set up to measure time interval between an event A (Start Event) and an event B (Stop Event). The time resolution of the count is limited strictly by the available time resolution of the counter.

Set the 168-D controls as follows.

Select Start and Stop events as desired, the former to the loop entrance statement address and the latter to the exit address. Set Delay to 0000.

| | |
|---|---|
| Record Mode: | Normal |
| | Normal |
| | µP |
| | ARM EXT |

Set the counter to measure time interval between two events, A and B. Connect the Start event output to the counter input A, and the Stop event output to counter input B. Reset the counter.

Arm the 168-D and reset the SUD. The counter will display the time required by the SUD to execute the loop selected by the Start and Stop events.

Figure 4.3 Memory display mode.

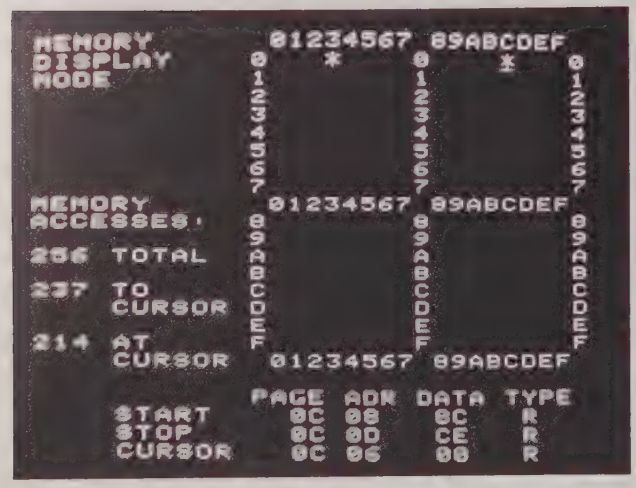



Figure 4.4 Memory display with cursor decremented from 215 to 214.

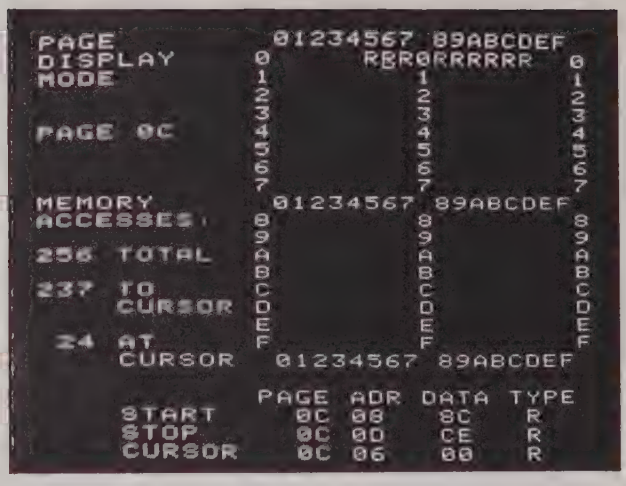



Figure 4.5 Page display mode.

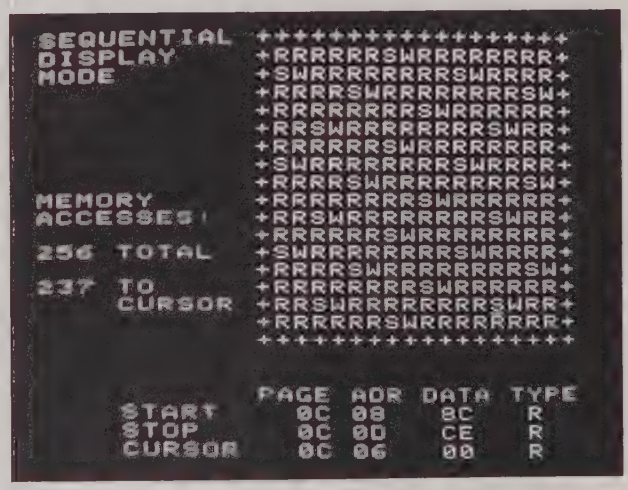



Figure 4.6 Sequential display mode. An S entry indicates all accesses with the same 16 bit address.

```
PAGE  ADR  DATA  TYPE
  03   FD    20     W
  0C   07    00     R
  0C   08    8C     R
  0C   08    8C     R
  0C   09    04     R
  0C   0A    00     R
  0C   0B    26     R
  0C   0C    F8     R
  0C   05    A7     R
  0C   06    08     R
  03   FE    20     W
  0C   07    08     R
  0C   08    8C     R
  0C   08    8C     R
  0C   09    04     R
  0C   0A    00     R
  0C   0B    26     R
  0C   0C    F8     R
  0C   05    A7     R
  0C   06    00     R

256 MEMORY ACCESSES
237 TO CURSOR
```

4.7 List display mode in hexadecimal.

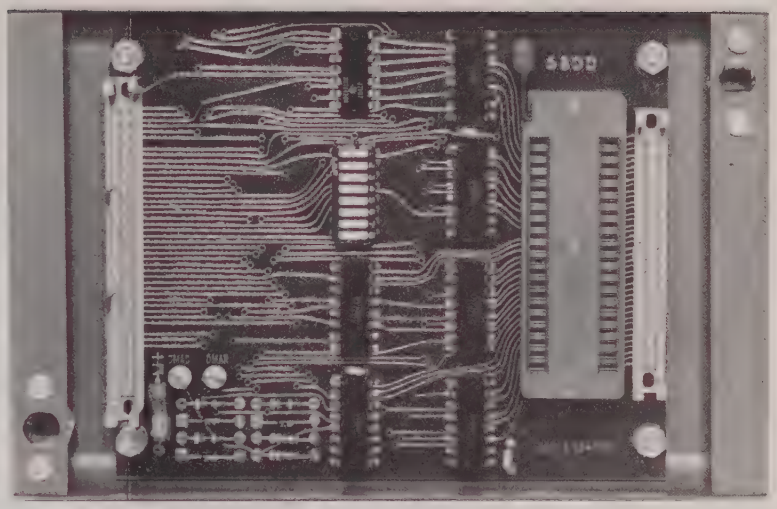


Figure 4.9 6800 personality module.

```
-ADDRESS------   --DATA---  R
0011  1111 1101   0010 0000  0
1100  0000 0111   0000 1000  1
1100  0000 1000   1000 1100  1
1100  0000 1000   1000 1100  1
1100  0000 1001   0000 0100  1
1100  0000 1010   0000 0000  1
1100  0000 1011   0010 0110  1
1100  0000 1100   1111 1000  1
1100  0000 0101   1010 0111  1
1100  0000 0110   0000 0000  1
0011  1111 1110   0010 0000  0
1100  0000 0111   0000 1000  1
1100  0000 1000   1000 1100  1
1100  0000 1000   1000 1100  1
1100  0000 1001   0000 0100  1
1100  0000 1010   0000 0000  1
1100  0000 1011   0010 0110  1
1100  0000 1100   1111 1000  1
1100  0000 0101   1010 0111  1
1100  0000 0110   0000 0000  1

  256 MEMORY ACCESSES
  237 TO CURSOR
```

e 4.8 List display mode in binary.

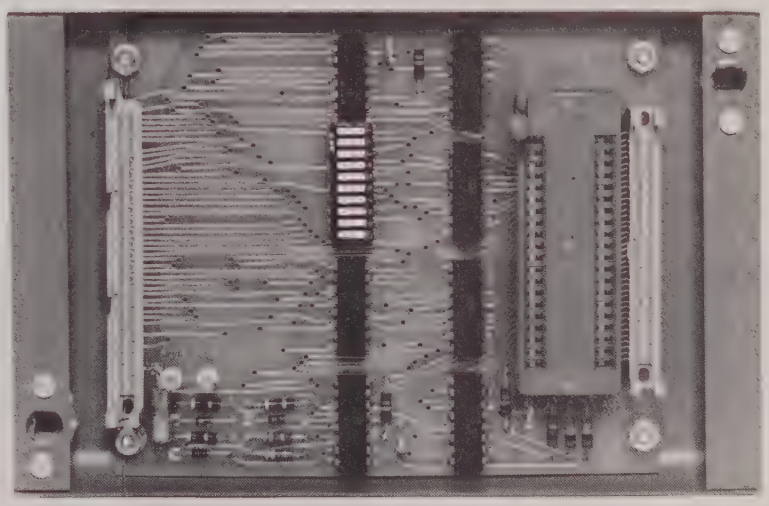


Figure 4.10 8080 personality module.

SOR

SECTION V

PERSONALITY MODULE INTERFACE

## 5.1 Introduction

This document describes the signals at the interface between the personality module and the 168-D, and how they are used in the 168-D for recording and control. Note that all signals are referenced to the 50-pin connector at the end of the ribbon cable emanating from the 168-D.

## 5.2 Electrical Characteristics at the Interface

### 5.2.1 Inputs to the 168-D

The load presented by the 168-D varies from one to five TTL inputs, depending upon which signal line is under consideration.

### 5.2.2 Output from the 168-D

The single output from the 168-D is a signal called $\overline{\text{SUDMPE}}$, which is a 7404 inverter output. It is used to control the microprocessor (MPU) in the SUD for single instruction execution.

## 5.3 Typical circuits in the Personality Module

### 5.3.1 Output Buffers

The outputs of the MPU in the system under development (SUD) are buffered using National DS8837 hex bus drivers/receivers. A typical address or data line is shown in Figure 5.1.

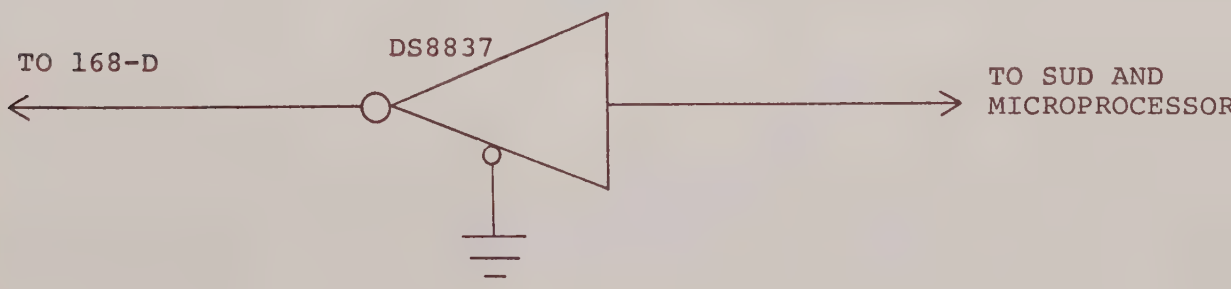



Figure 5.1 Typical Address/Data Buffer

The maximum input current to the DS8837 is 50 μA (typically 15 μA). The output is rated for a fanout of 10 TTL loads.

### 5.3.2 Input Buffers

The input to the MPU in the SUD is buffered using a 74126. The circuit is shown in Figure 5.2.

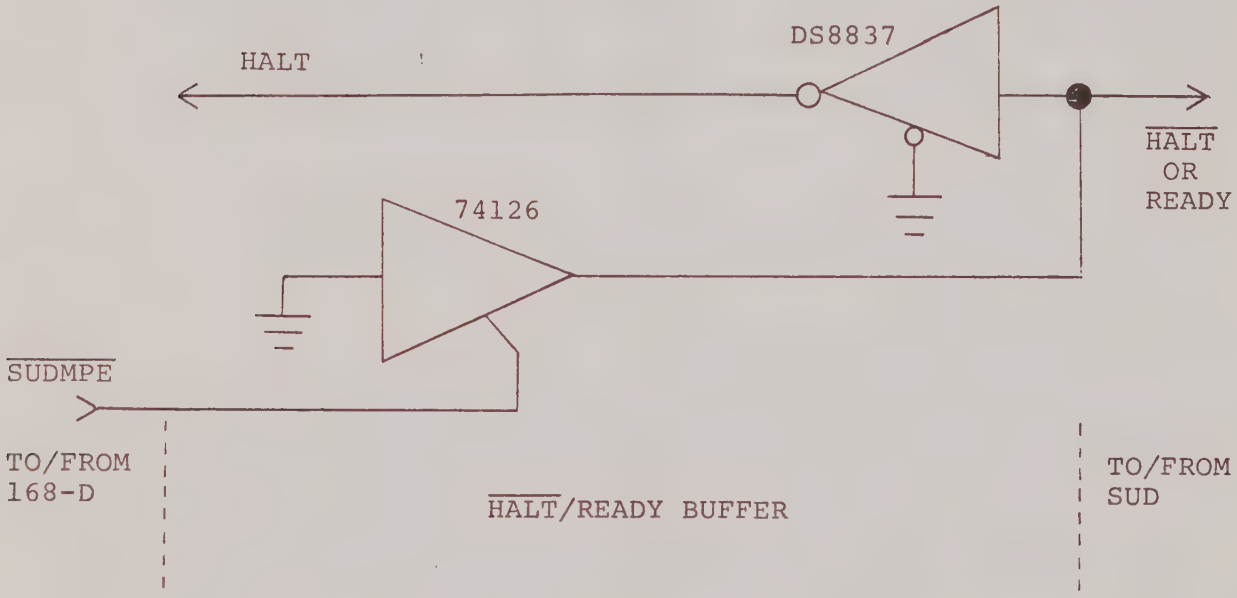



Figure 5.2 74126 Circuit

The MPU in the SUD is enabled (normal operation) when SUDMPE is low. During single instruction execution, SUDMPE is held high and pulsed low for one clock cycle. The edge of the Ø1 clock is used to control SUDMPE. Also see Section 5.5.

## 5.4 Recording Process

### 5.4.1 Selection Between MPUs

The 168-D tells whether the personality module is attached to an 8080 or a 6800 type MPU by the state of the SUD1C LINE: SUD1C is high for a 6800 and low for an 8080.

### 5.4.2 Recording when SUDIC is High

The address lines of the SUD are compared with either the Start event or the Stop event during the positive duration of the SUD Ø2 clock. If they compare, a record clock is generated, and the data is stored. Recording is further qualified using the $\overline{\text{SUDVMA}}$ line being low. See Figure 5.3.

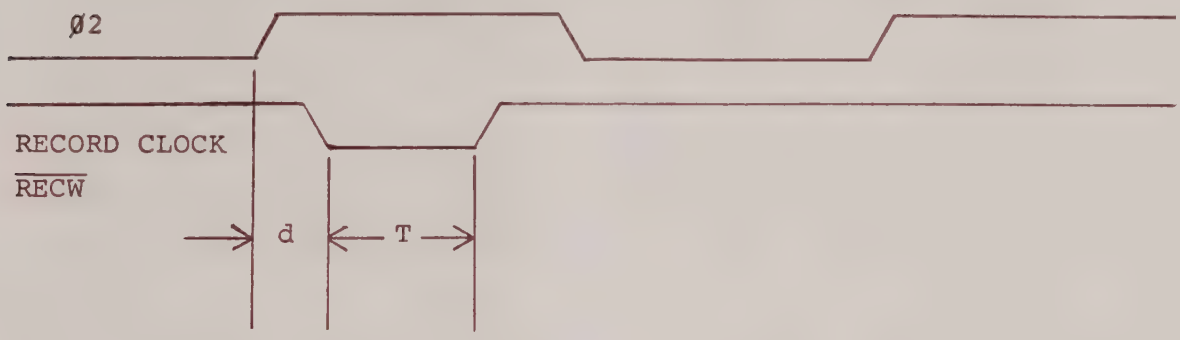



Figure 5.3 Recording 6800 Data

The compare operation occurs during the Ø2 clock. The width of the record clock (T) is determined by the delay through the three inverter paths in Figure 5.4.

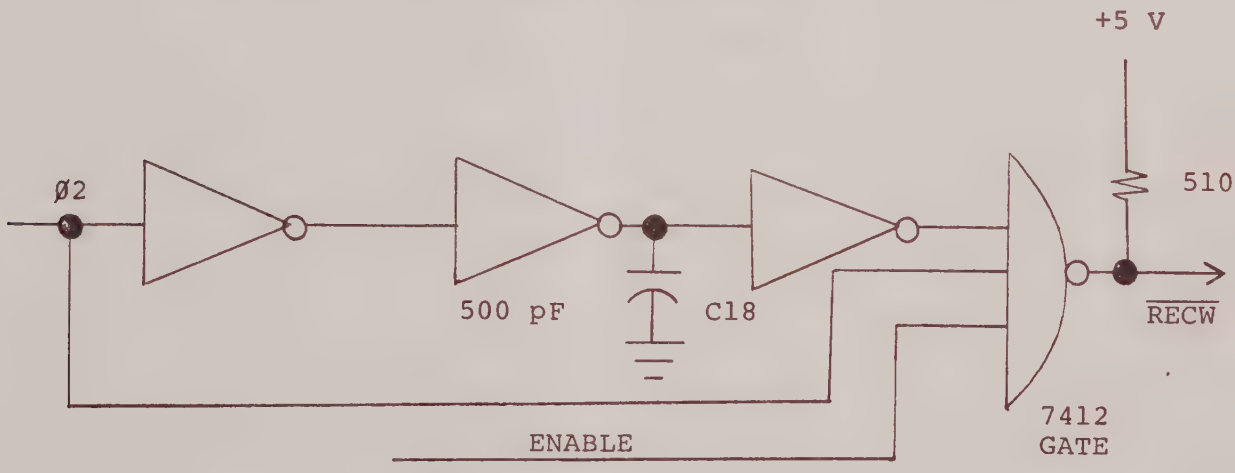



Figure 5.4 6800 Record Circuit

The delay (d) is the propagation delay through the 7412 gate. The reason the record clock was generated from the rising edge of the Ø2 clock is that some development systems (e.g. Motorola Exorciser) stretch the Ø2 clock when cycle stealing or dynamic memory refreshing is done. The wrong data would be recorded if the entire width of the Ø2 clock were used for recording. The user may change the width of the record clock by changing the value of C18 on the Record Control PCB.

### 5.4.3 Recording when SUD1C is low

The comparison is identical to that shown in Figure 5.3. However, the entire width of the Ø2 clock is used for recording.

In addition, the status of the 8080 is recorded if SWSTAT is high. This is done using the positive duration of the Ø1 clock during the time that SYNC is low (SYNC is high).

### 5.4.4 Recording DMA Events

The states of the address, data, and Read/Write lines can be recorded using the SUDMAC (Direct Memory Access Clock) and SUDMAR (Direct Memory access Request) inputs to the 168-D.

The record clock is generated using the rising edge of the DMAC signal and occurs approximately 30 nsec after DMAC goes high.

A DMA access cannot be a Start or a Stop event. The external Start and Stop BNC inputs (on the 168-D) should be used for observing only DMA activity.

## 5.5 Signal Pinouts and Specifications

Table 5.1 describes the signals and levels required for proper operation with any given MPU. All levels are TTL (high = +3.5 V, low = 0.7 V). Signals are referenced to the 50-pin connector at the end of the ribbon cable emanating from the 168-D.

Table 5.1 Signal Pinouts and Specifications

| Pin No. | Signal Name 6800 | 8080 | Gen'l Name | Input/ Output | High/Low Active | Functional Description |
|---|---|---|---|---|---|---|
| 1 | HALT | $\overline{\text{READY}}$ | HALT | I | HI | Sense line. Allows 168-D to check status of SUD MPU Halt line. If high, 168-D will not halt SUD MPU.<br><br>SUD Halt or Ready line must be pulled up (within SUD) through an approximately 2.2 kΩ resistor so that 168-D can pull it to a low level when required. |
| 2 | NO CONNECTION | | | | | |
| 3 | | | $\overline{\text{SUDMPE}}$ | O | LO | Normally low. Goes high in Halt record mode to halt SUD MPU. Pulsed low to enable single instruction execution.<br><br>For single cycle MPUs (i.e., 6800), SUDMPE goes low on rising edge of first Ø1 clock pulse immediately following pressing SINGLE button (13). Stays low for one Ø1 clock cycle.<br><br>For multicycle MPUs (i.e., 8080), $\overline{\text{SUDMPE}}$ goes low as above, and stays low until |

| Pin No. | Signal Name 6800 | 8080 | Gen' Name | Input/ Output | High/Low Active | Functional Description |
|---|---|---|---|---|---|---|
| | | | | | | next Fetch is signified by ANDing of SUD5 (pin 28) and $\overline{SYNC}$ (pin 36). |
| 4 | NO CONNECTION | | | | | |
| 5 | $\overline{VMA}$ | $\overline{DBIN}$ | $\overline{SUDVMA}$ | I | LO | When low, enables 168-D compare for Start/Stop event and enables record clock. |
| 6 | NO CONNECTION | | | | | |
| 7 | - | - | $\overline{SUDMAA}$ | | | Not used. |
| 8 | VCC | +5 V | +5 V PWR | O | | Available current is 400 mA, with NO Personality Module connected. |
| 9 | $\overline{SUA\emptyset}$ | $\overline{SUA\emptyset}$ | $\overline{SUA\emptyset}$ | I | LO | Address $2^0$ (LSB) |
| 10 | $\overline{SUA1}$ | $\overline{SUA1}$ | $\overline{SUA1}$ | I | LO | Address $2^1$ |
| 11 | $\overline{SUA2}$ | $\overline{SUA2}$ | $\overline{SUA2}$ | I | LO | Address $2^2$ |
| 12 | $\overline{SUA3}$ | $\overline{SUA3}$ | $\overline{SUA3}$ | I | LO | Address $2^3$ |
| 13 | $\overline{SUA4}$ | $\overline{SUA4}$ | $\overline{SUA4}$ | I | LO | Address $2^4$ |
| 14 | $\overline{SUA5}$ | $\overline{SUA5}$ | $\overline{SUA5}$ | I | LO | Address $2^5$ |
| 15 | $\overline{SUA6}$ | $\overline{SUA6}$ | $\overline{SUA6}$ | I | LO | Address $2^6$ |
| 16 | $\overline{SUA7}$ | $\overline{SUA7}$ | $\overline{SUA7}$ | I | LO | Address $2^7$ |
| 17 | $\overline{SUA8}$ | $\overline{SUA8}$ | $\overline{SUA8}$ | I | LO | Address $2^8$ |

| Pin No. | Signal Name 6800 | 8080 | Gen'l Name | Input/ Output | High/Low Active | Functional Description |
|---|---|---|---|---|---|---|
| 18 | $\overline{SUA9}$ | $\overline{SUA9}$ | $\overline{SUA9}$ | I | LO | Address $2^9$ |
| 19 | $\overline{SUA1Ø}$ | $\overline{SUA1Ø}$ | $\overline{SUA1Ø}$ | I | LO | Address $2^{10}$ |
| 20 | $\overline{SUA11}$ | $\overline{SUA11}$ | $\overline{SUA11}$ | I | LO | Address $2^{11}$ |
| 21 | Ø | RECORD STATUS | SWSTAT | I | HI | Enables recording of 8080 status at SYNC time. |
| 22 | $\overline{SUA12}$ | $\overline{SUA12}$ | $\overline{SUA12}$ | I | LO | Address $2^{12}$ |
| 23 | $\overline{SUA13}$ | $\overline{SUA13}$ | $\overline{SUA13}$ | I | LO | Address $2^{13}$ |
| 24 | $\overline{SUA14}$ | $\overline{SUA14}$ | $\overline{SUA14}$ | I | LO | Address $2^{14}$ |
| 25 | $\overline{SUA15}$ | $\overline{SUA15}$ | $\overline{SUA15}$ | I | LO | Address $2^{15}$ MSB |
| 26 | $\overline{SUD7}$ | $\overline{SUD7}$ | $\overline{SUD7}$ | I | LO | Data $2^7$ MSB |
| 27 | $\overline{SUD6}$ | $\overline{SUD6}$ | $\overline{SUD6}$ | I | LO | Data $2^6$ |
| 28 | $\overline{SUD5}$ | $\overline{SUD5}$ | $\overline{SUD5}$ | I | LO | Data $2^5$ |
| 29 | $\overline{SUD4}$ | $\overline{SUD4}$ | $\overline{SUD4}$ | I | LO | Data $2^4$ |
| 30 | $\overline{SUD3}$ | $\overline{SUD3}$ | $\overline{SUD3}$ | I | LO | Data $2^3$ |
| 31 | $\overline{SUD2}$ | $\overline{SUD2}$ | $\overline{SUD2}$ | I | LO | Data $2^2$ |
| 32 | $\overline{SUD1}$ | $\overline{SUD1}$ | $\overline{SUD1}$ | I | LO | Data $2^1$ |
| 33 | $\overline{SUDØ}$ | $\overline{SUDØ}$ | $\overline{SUDØ}$ | I | LO | Data $2^0$ LSB |
| 34 | $\overline{SUDR}$ | $\overline{SUDR}$ | $\overline{SUDR}$ | I | | Defines a Read or Write operation: Low to Read, high to Write. |

| Pin No. | Signal Name 6800 | 8080 | Gen'l Name | Input/ Output | High/Low Active | Functional Description |
|---|---|---|---|---|---|---|
| 35 | NO CONNECTION | | | | | |
| 36 | | $\overline{\text{SYNC}}$ | $\overline{\text{SYNC}}$ | I | LO | Low level indicates that a multicycle MPU is at the beginning of a major machine cycle. Required for single step recording and for recording MPU status bytes. |
| 37 | NO CONNECTION | | | | | |
| 38 | NO CONNECTION | | | | | |
| 39 | $\overline{\text{SUD1C}}$ | $\overline{\text{SUD1C}}$ | $\overline{\text{SUD1C}}$ | I | | Set high for a single cycle MPU (i.e., 6800). Set low for a multicyle MPU (i.e., 8080). |
| 40 | NO CONNECTION | | | | | |
| 41 | NO CONNECTION | | | | | |
| 42 | $\overline{\text{DMAR}}$ | $\overline{\text{DMAR}}$ | $\overline{\text{SUDMAR}}$ | I | LO | Low when a SUD peripheral requests memory bus. |
| 43 | $\overline{\text{DMAC}}$ | $\overline{\text{DMAC}}$ | $\overline{\text{SUDMAC}}$ | I | LO | Clock for DMA operation |
| 44, 45, 46, 47, 50 | GND | GND | GND | | | Power and logic return. |
| 48 | $\overline{\text{SUDCP1}}$ | $\overline{\text{SUDCP1}}$ | $\overline{\text{SUDCP1}}$ | I | LO | SUD clock Ø1 |
| 49 | $\overline{\text{SUDCP2}}$ | $\overline{\text{SUDCP2}}$ | $\overline{\text{SUDCP2}}$ | I | LO | SUD Clock Ø2 |

# SECTION VI

# CALIBRATION PROCEDURE

## 6.1 Introduction

The Model 168-D Microprocessor Analyzer, as with all electronic equipment manufactured by Biomation, has in accordance with the manufacturing procedure experienced extensive testing. Although the system was calibrated prior to shipment, recalibration of the internal circuits are recommended on a periodic basis, averaging approximately once every six months.

This section contains the procedures for calibrating the 168-D analyzer. These procedures should be followed as presented herein to achieve the desired operating response from the system.

## 6.2 Suggested Test Equipment and Test Aids

The following test equipment are recommended for calibration and service of the Model 168-D Microprocessor Analyzer.

1. Oscilloscope (DC to 100 MHz, dual channel).
2. Digital voltmeter (4-1/2 digit DVM).
3. Function generator (Must supply a triangle waveform at 50 kHz and 5 V p-p).
4. Frequency counter.
5. 6800 SUD.
6. 6800 personality module.
7. Shift program.
8. Tuning tool.
9. Six-inch screw driver with insulating sleeving on the shank.
10. IC clip.
11. BNC-T adaptor.

## 6.3 Power Supply Calibration

Be sure the AC power is off. Remove the top cover. Refer to Section VIII under disassembly procedures. Remove the MPU PCB. See Section IX, Figure 9.24, PCB location. Remove the extender board. Place the extender board in the MPU PCB slot.

Mount the MPU PCB on the extender board. Turn on the AC power. Let the system stabilize for five minutes before making adjustments. Connect the DVM's common lead to I/O pin 99 or 100. See Figure 9.9, MPU PCB schematic. Monitor the test point with the positive lead. Adjust the corresponding controls on the power supply PCB to obtain the values as defined in Table 6.1. See Figure 9.26 for the control locations for the various supplies.

Table 6.1 Power Supply Adjustments

| Adjustment | Voltage | Monitor at MPU PCB |
|---|---|---|
| +5 V | +5.0 V ± 0.1 V | 1 I/O 1,2 |
| +12 V | +12.0 V ± 0.1 V | 2 I/O 5,6 |
| +12 V | -12.0 V ± 0.5 V | 3 I/O 7,8 |

Measure the -5 V supply at the cathode of CR2, TP4. It should be -5 V ±0.25 V. Replace CR2 if the -5 V supply is out of specification and the -12 V supply is correct.

## 6.4 Oscillator Calibration

See Figure 9.9, MPU PCB schematic. Monitor TP5 (K8-4) with the frequency counter. The frequency should be 22.008 MHz ±0.002 MHz. Adjust C29 to obtain the correct frequency. Turn the AC power on the 168-D off/on. Verify that the oscillator remains on frequency. Replace the MPU card back into its slot after calibrating the oscillator.

## 6.5 Interim Calibration Review

Before continuing with the CRT display calibration, READ this section thoroughly.

The CRT display must use high voltages because of its principle of operation. These high voltages present potential shock hazards to the inexperienced and careless service person. Review Figure 9.27, CRT Display section, as it shows exposed high voltage points that are close to or a function of adjustments to be performed.

CRT display calibration procedures introduced by Biomation are intended to provide the user of the 168-D with quick methods for adjusting the display section according to personal preference in the desired character presentation.

The following are a summary of the adjustments: focus adjust, brightness adjust, contrast adjust, vertical size adjust, vertical linearity adjust, vertical hold adjust, horizontal hold adjust, centering adjust, and horizontal/vertical deflection adjust.

Presented in Section VIII is a more indepth circuit analysis and maintenance procedure for the 168-D. The CRT display has a separate section (see Appendix B) that was prepared by the manufacturer of the CRT. It is recommended that this section be reviewed for a more detailed analysis of the CRT display.

### 6.5.1 Safety Precautions

The following are basic safety precautions to observe while performing the calibration on the CRT display section. Failure to observe these precautions could result in electrical shock that could be fatal or cause bodily injury.

1. Review the available documentation in Section IX and Appendix B on the potential shock hazards in the CRT display section.

2. Use insulated tuning tools.

3. Remove all jewelry (rings, watches, neck chains, etc).

4. Use only one hand while touching or tuning the CRT display. Keep the other hand in your rear pocket.

5. Exercise patience while making adjustments.

6. Turn the system off if the tuning tool falls to the circuit board before attempting to pick it up.

## 6.6 CRT Display Calibration

The following adjustments are made at the discretion of the user.

Adjustments on the CRT display can be made with the 168-D operating in a normal analytical environment. The test examples presented are intended to show the undesired as compared to the desired response of the CRT display as defined by Biomation standards. To compare the field system to lab generated results, remove the 168-D from the analytical test configuration. Connect the following items if they are not already connected to the 168-D.

1. 6800 personality module.

2. 6800 SUD with an installed shift program.

6.6.1 Focus Adjust (R61) [POTENTIAL SHOCK HAZARD]

Acquire the following switch settings.

| Switch | Position |
|---|---|
| Start Event Source | Event |
| Start Event Mode | Read |
| Start Event Page | 0C |
| Start Event Address | 00 |
| Delay | 0000 |
| Delay Modifier | Start |
| Stop Event Source | Event |
| Stop Event Mode | Read |
| Stop Event Page | 0C |
| Stop Event Address | 10 |
| Record Select | Normal |
| Record Control | Normal |
| Display Select | List |
| Access | µP |
| AC Power | ON (up) |

Manually arm the 168-D. Reset the SUD. Verify that the data format on the CRT compares to Figure 6.1A. Depress the Normal/Select to Select. Observe that the data is now presented in a digital format. See Figure 6.1B. Refer to Figure 9.27, CRT display section, for the adjustment control location for the CRT display section. Observe the CRT display and adjust the Focus control (R61) to sharpen the characters. For best results, adjust the characters in the center of the CRT.

6.6.2 Brightness Adjust (R63) [POTENTIAL SHOCK HAZARD]

Using the same display format as above, adjust the brightness control (R63) to increase or decrease the brightness of the characters.

6.6.3 Contrast Adjust (R5) [CAUTION]

Maintain the digital display format. The contrast, brightness and video bias controls interact to affect the brightness of the characters, cursor, and raster.

The contrast tends to decrease the brightness of the cursor in relation to the character, along with controlling the black/white response.

Adjusting the contrast control to decrease the contrast

also decreases the brightness of the display. It also decreases the brightness of the cursor in relation to the brightness of the character. It is necessary to increase the brightness of the total display using the brightness control. See Section VII (7.3.2.1) for explanations regarding characters and cursor presentation on the CRT.

See Figure 6.1C. Here contrast is decreased and the brightness is increased. The cursor appears equal to the character. See Figure 6.1D. Here the contrast is increased and the brightness control is adjusted to bring down the brightness. The cursor appears much brighter compared to the characters.

Adjust the contrast control to have the cursor slightly brighter than the characters.

6.6.4 Vertical Size Adjust (R52) [CAUTION]

Maintain the digital display format. Adjust the vertical height of the display format using the vertical size adjust (R52).

6.6.5 Vertical Linearity Adjust (R57) [CAUTION]

Switch the Normal/Select switch to normal (List mode). Observe Figure 6.1A. Observe Figures 6.1E,F. Adjusting the vertical linearity control affects the vertical drive ramp. Adjust the vertical control to make the characters equal in size from both top and bottom.

6.6.6 Vertical Hold Adjust (R49) [CAUTION]

Observe the List mode. See Figure 6.1G. This is an example of the display rolling over on itself. This type of response should normally not occur. However, if it does occur adjust the vertical hold control (R49).

6.6.7 Horizontal Hold Adjust (R35) [CAUTION]

Observe the List mode. See Figures 6.1H,I as it depicts the horizontal hold adjust (R35) being out of adjustment. This control affects the variable charge current, which assists in determining the horizontal frequency of the oscillator. The test examples show the type of response that results when the horizontal frequency starts to loose synchronization. Adjust this control to position the characters at a 90 degree angle to the horizontal plane. See the example below. After adjusting, turn the system OFF/ON. The display should be readable. If the horizontal hold adjust is incorrect, the display might be as in Figure 6.1I. Repeat the adjustment. If the system still comes up as depicted in 6.1I, see Figure 6.1H and measure the oscillator frequency.

6.6.8 Centering Adjust [SHOCK HAZARD]

Observe the digital display mode. See Figure 6.1J. Disregard the omission of the complete display format. Direct your attention to the lower left-hand corner of the photograph. Observe the out-of-focus appearance of the "O" characters in that area. Observe Figure 6.1K. This figure represents the desired CRT display. Adjust the center adjust to correct for the display format being off center. Position the display that is in the center of the CRT screen.

6.6.9 Horizontal/Vertical Deflection [SHOCK HAZARD]

Observe the List display mode. See Figure 6.1L. Notice how the display is rotated. Adjust the yoke to correct for this type of response. See Figure 9.27, CRT adjustments.

## 6.7 Threshold Circuit Calibration (168-D)

Turn the AC power off on the 168-D. Adjust the function generator for the following conditions using the oscilloscope:

Frequency - 50 kHz.

Waveform - Triangle pattern.

Amplitude - 8 V p-p.

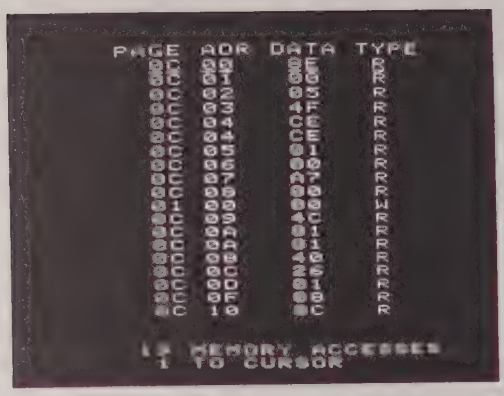
Connect the BNC-T adaptor to the output of the generator. Connect one side to the oscilloscope and the other side to the ARM BNC input of the 168-D. Place the Record Control board on the extender board. Observe TP1 at C5-13. This input comes from the Front Panel board U16-4 (J10-6) and is the External Arm Output (EXARM). See Figure 9.5A and notice the following scope settings: vertical is 1 V/cm, horizontal is 2 µsec/cm, Channel 1 is the input waveform, and Channel 2 is the EXARM (C5-13) input waveform on the Record Control PCB.

Adjust R27 to adjust the trigger level on the input waveform at 3 V. See Figure 9.5 for the front panel schematic and Figure 9.25 for the location of R27.

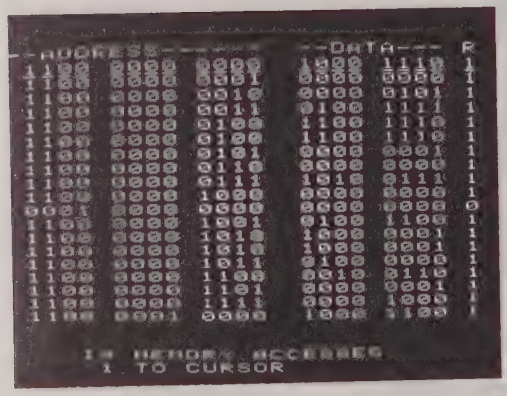
Connect CH 1 to record control card pin 24. Verify that the output pulse width of J10-7 varies as a function of each of the following conditions: Place threshold to variable and adjust threshold pot, threshold X1, and

threshold X10 (10X > 1), and change start slope from positive to negative, observing that logic one/zero levels invert. (U15-6 is a logical nonlinear waveform.)

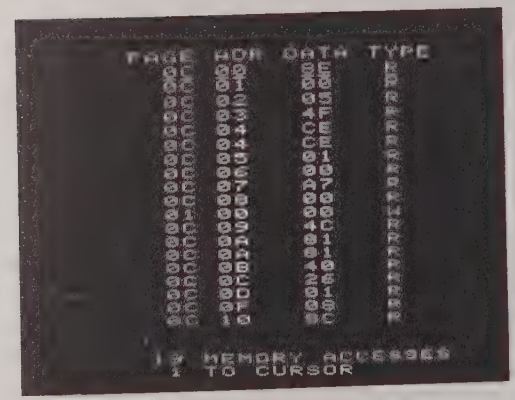
Connect scope CH 1 to record control card pin 25 and function generator output to MPA stop event input. Repeat the above procedure using threshold and stop slope, verifying functional waveforms.


PAGE ADR DATA TYPE
19 MEMORY ACCESSES
1 TO CURSOR

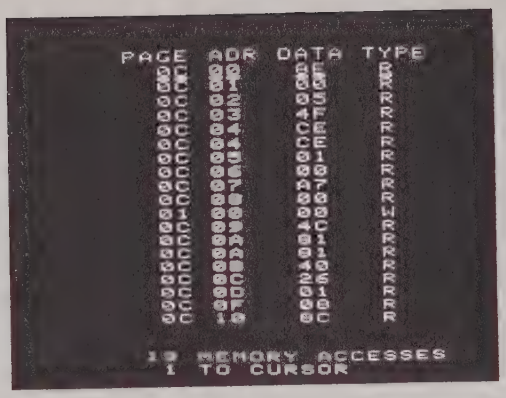
A.


--ADDRESS-------- --DATA--- R
19 MEMORY ACCESSES
1 TO CURSOR

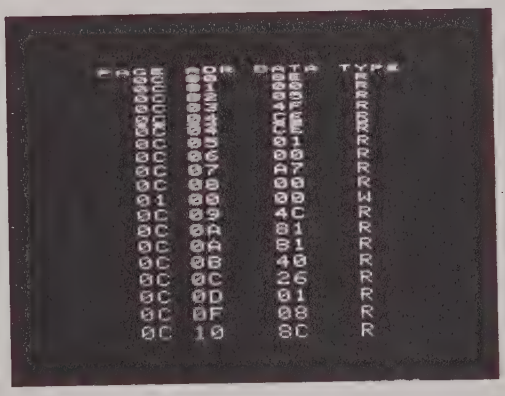
B.


PAGE ADR DATA TYPE
19 MEMORY ACCESSES
1 TO CURSOR

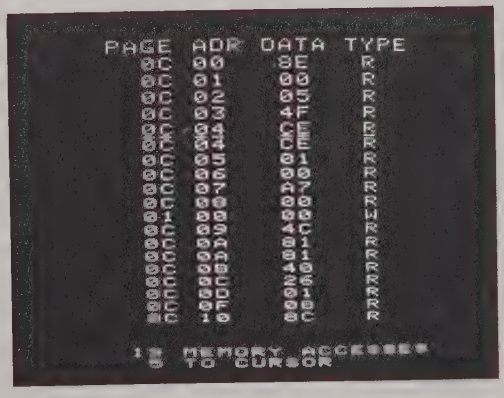
C.


PAGE ADR DATA TYPE
19 MEMORY ACCESSES
1 TO CURSOR

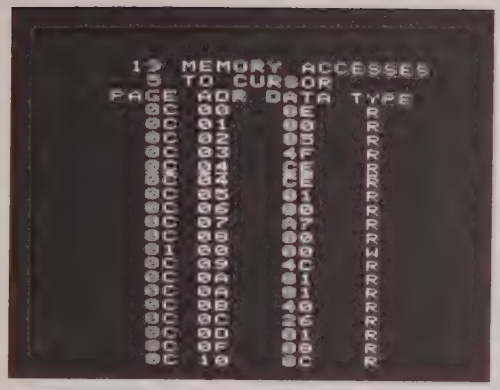
D.



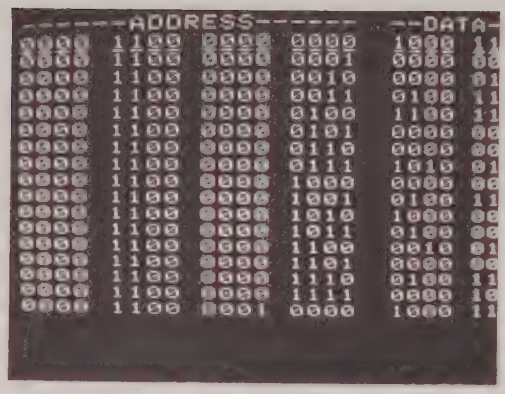
E.


PAGE ADR DATA TYPE
19 MEMORY ACCESSES
5 TO CURSOR

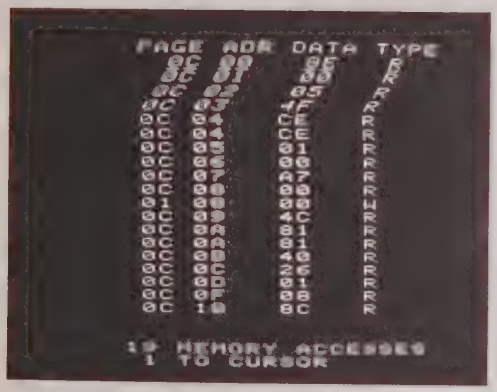
F.




G.



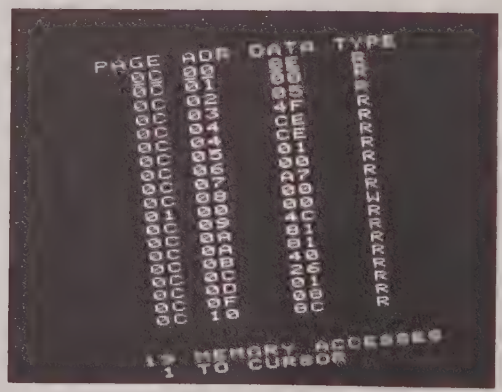

J.




H.

K.

I.




L.

Figure 6.1 Waveform Photographs

# SECTION VII

# TECHNICAL DESCRIPTION

## 7.1 Introduction

The Microprocessor Analyzer may be described on a functional basis in terms of five blocks. These blocks are:

1. The Microprocessor Unit (MPU) with its RAM and ROM
2. The CRT Driver and Monitor
3. The Record Processor
4. The Control Panel
5. The Personality Module

The MPU, CRT Driver, and Record Processor consist of electronic solid-state circuits that are located on four printed circuit boards (PCBs) and which are interconnected by means of a fifth PCB, which is called the Motherboard. These cards are held in a card cage.

The Control Panel consists of the physical panel, switches and indicators (light-emitting diodes or LEDs), and solid-state circuits that are mounted on a PCB located just behind the control panel.

The CRT Monitor consists of a 9-in. CRT and associated solid-state electronic circuits. These circuits perform two basic functions. One group amplifies the composite video signal and drives the electron beam. The other group converts the +12 supply voltage to +9,500 V for use as an accelerating voltage for the cathode of the CRT. The CRT Monitor is purchased as a complete unit from Motorola Display Products.

The Personality Module consists of a PCB, solid-state buffers and drivers, and miniature DIP switches.

## 7.2 General Functional Description

### 7.2.1 Information Flow

The flow of information between the functional blocks of the MPA can be most easily understood by referring to Figure 7.1.

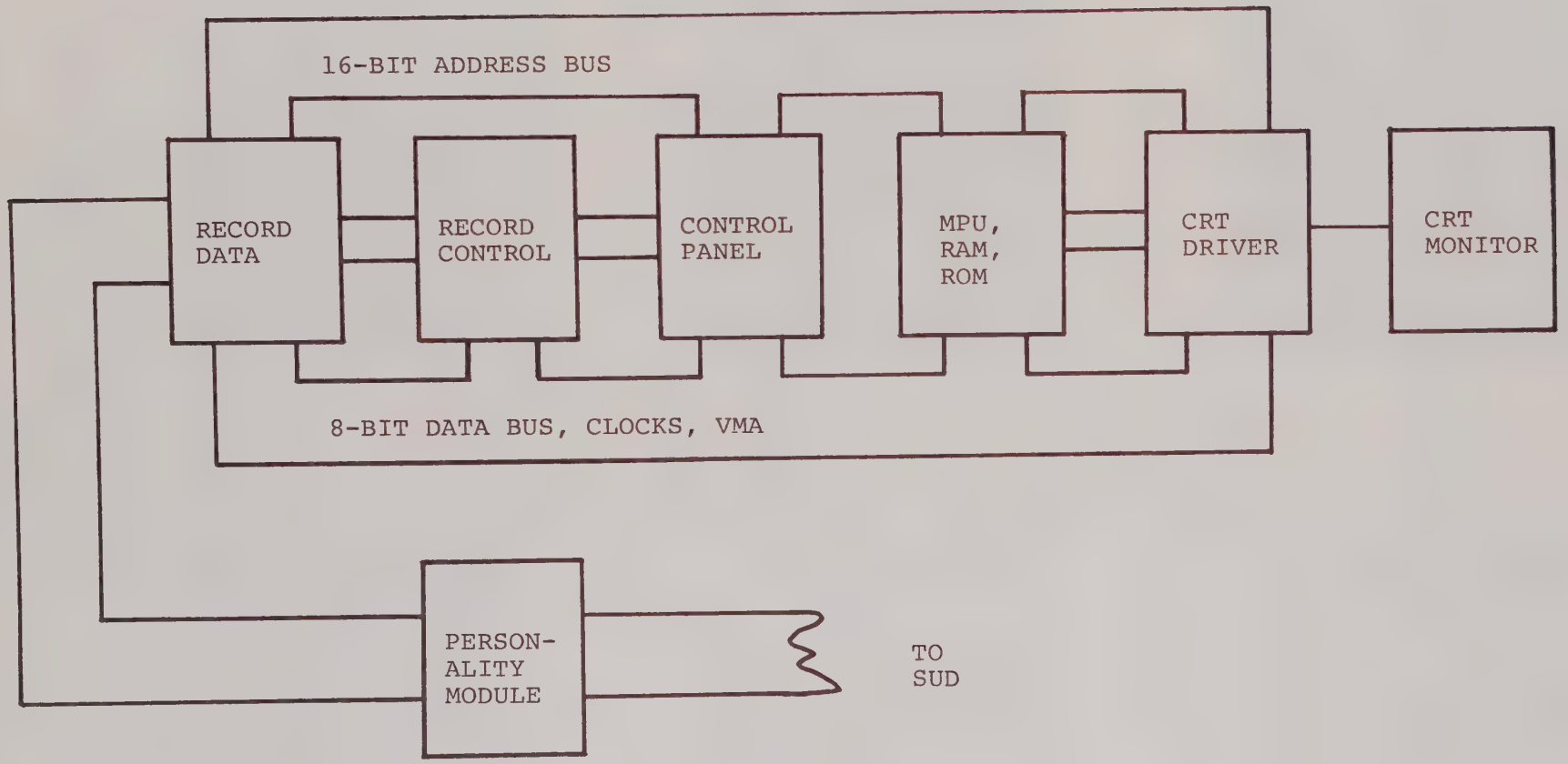



Figure 7.1 168-D Block Diagram

#### 7.2.1.1 MPU and CRT Driver

The MPU causes data to be presented to the operator by writing it in the appropriate locations in RAM. The CRT driver reads these RAM locations at the proper time and generates a composite video signal to drive the CRT Monitor.

The CRT driver requests control of the RAM Memory by causing the Direct Memory Access Request (DMAR) control line to go low. The MPU acknowledges the request by causing the bus available (MPBA) line to go high. A line of 32 characters is then loaded from RAM into the line buffer during an inactive scan line. The 32 data characters are recirculated for nine scan lines, during which time they are "painted" on the CRT. The process is repeated to present 24 lines of 32 characters each. The CRT screen is refreshed 60 times each second.

#### 7.2.1.2 MPU and Control Panel

The MPU communicates with the appropriate switches on the control panel by writing different data into memory location 2000 (Hexadecimal) and then reading from the same location.

#### 7.2.1.3 MPU and Record Processor

The MPU communicates with the Record Processor by reading its status (2001) and loading control and data words into latches. In addition, the MPU has the ability to read the contents of the Record Buffer and the address counter, which is used to determine where to write in the Record Buffer.

After determining that the Record Processor is armed, the MPU loads control and data words into it and thus causes it to search for a start event. After finding the start event, recording, and finding the stop event, the Record Processor stops recording and signals the MPU that the Record Buffer contains valid data. The MPU then reads the data from the Record Buffer and presents it in the display format specified by the operator.

#### 7.2.1.4 Record Processor and Personality Module

The Record Processor monitors the outputs of the Personality Module while searching for a start event, recording, and searching for a stop event. The only signal that flows from the Record Processor to the Personality Module is the line that controls single instruction execution.

### 7.2.2 Memory Organization

The memory map of the MPA is shown in Figure 7.2.

| TYPE | BASE 10 | BASE 16 | DESCRIPTION |
|---|---|---|---|
| 2.5K ROM | 5119 | 11FF | Program ROM 512 X 8 2704 |
| | 4096 | 1000 | |
| | 4095 | 0FFF | Program ROM 1K X 8 2708 |
| | 3072 | 0C00 | |
| | 3071 | BFF | Program ROM 1K X 8 2708 |
| | 2048 | 800 | |
| 1K X 8 OR 256 X 25 RAM | 2047 | 7FF | Record Buffer 256 X 25 27LS01 |
| | 1024 | 400 | |
| 1K X 8 RAM 2102 | 1023 | 3FF | Display Screen 768 locations |
| | 256 | 100 | |
| | 255 | FF | Work Storage 256 X 8 |
| | 0 | 0 | |

NOTE: Peripherals are addressed when A13 = 1 and A12 = 0, i.e., addresses $2XXX_{16}$.

Figure 7.2 168-D Memory Map

Memory is divided into four general areas: MPU RAM, Record Buffer RAM, ROM, and peripherals, which appear as memory locations to the MPU.

7.2.2.1 MPU RAM

The lower 1024 bytes of memory are designated as MPU RAM. These eight 2102 RAMs are located on the MPU PCB. The 6800 can read from and write into this RAM. The CRT driver reads from locations 100 through 3FF and displays the data in these locations on the CRT screen. The lower 256 bytes are used by the 6800 for storage of temporary data (e.g., switch positions) and program variables.

The organization of the display screen is shown in Figure 7.3. The screen is organized as 24 lines of 32 characters each. The upper left-hand corner of the screen is address 100 and the lower right-hand corner of the screen is address 3FF.

7.2.2.2 Record Buffer

The second 1024 bytes of RAM (as addressed by the 6800) are locations 400 through 7FF. The MPU can only read these locations; it cannot write into them.

During the recording process, the Record Processor writes into this RAM as 256 words of 25 bits each. This RAM is mechanized as 25 256 X 1 RAMs and is located on the Record Data PCB. The organization of data within the Record Buffer, assuming a full buffer, is as shown in Figure 7.4. In this figure, AU (8 bits) represents the upper 8 bits of the SUD address, AL (8 bits) the lower 8 bits of the SUD address, D (8 bits) the SUD data, and R/W (1 bit) the SUD Read/Write Line. The data in the Record Buffer is recorded such that when it is read by the 6800, the most significant bit is leftmost. The Read/Write bit appears as the most significant bit of data in the appropriate addresses.

Note that for brevity, not all addresses are shown.

7.2.2.3 ROM

The system operating program is stored in ROM beginning at location 800 and ending at location 11FF. The last location used is 11EB. The ROM is mechanized using two 2708s and one 2704; the 2704 is the upper 512 bytes. The ROM is located physically on the MPU PCB.

When power is applied to the MPA or when the CLEAR switch is activated, the 6800 puts FFFE on the address bus and reads the data on the data bus into the most significant 8 bits of its program counter. The second operation the 6800 performs is reading the data at location FFFF into the least significant 8 bits of its program counter. In the

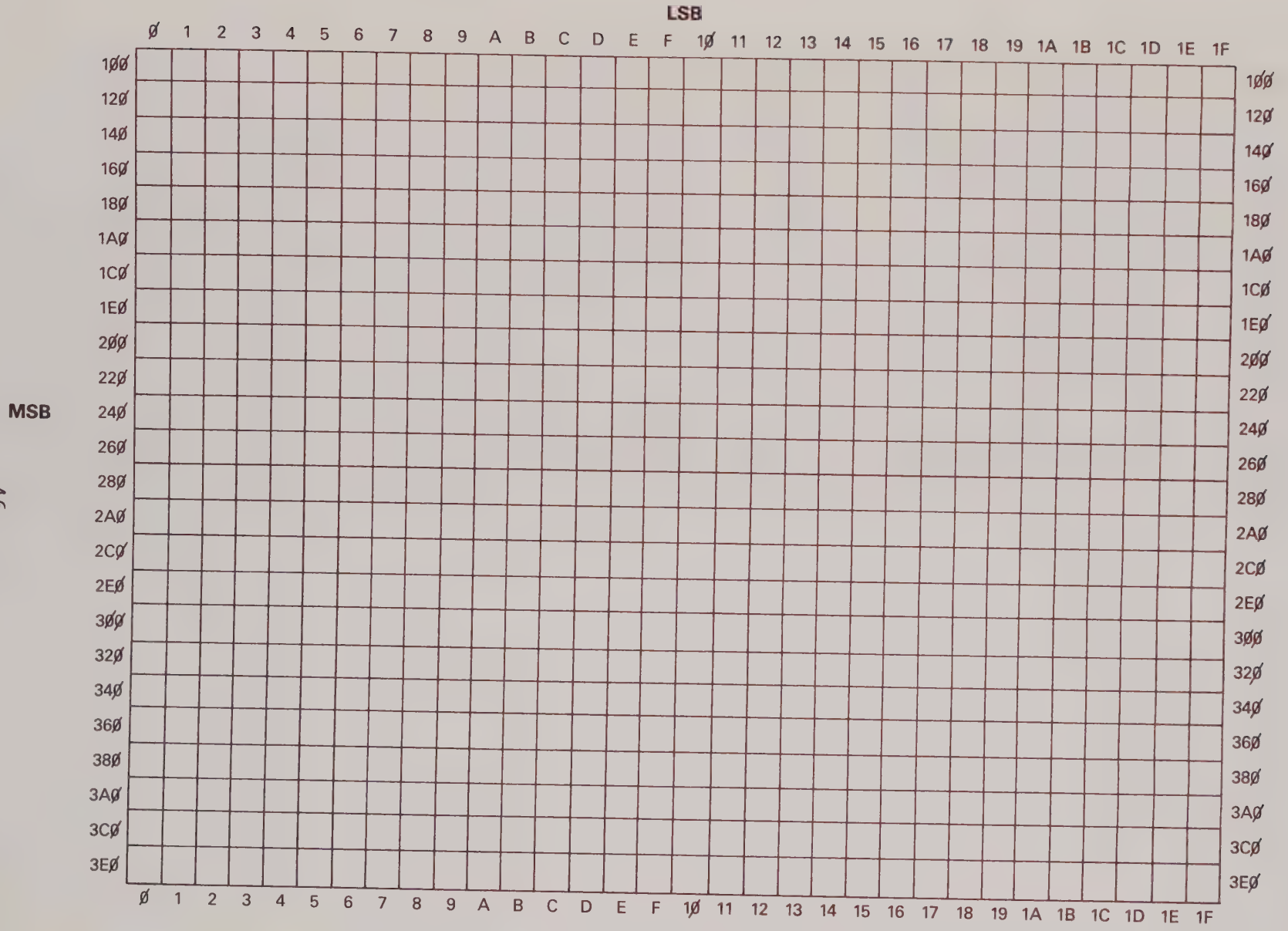



Figure 7.3 Display Screen

| ADDRESS READ BY MPU (+400) | | | | | ADDRESS WHEN RECORDING | SAMPLE NO. |
|---|---|---|---|---|---|---|
| 0 | 1 | 2 | 3 | | 0 | 1 |
| 4 | 5 | 6 | 7 | | 1 | 2 |
| 8 | 9 | A | B | | 2 | 3 |
| C | D | E | F | | 3 | 4 |
| 10 | 11 | 12 | 13 | | 4 | 5 |
| 14 | 15 | 16 | 17 | | 5 | 6 |
| 18 | 19 | 1A | 1B | | 6 | 7 |
| 1C | 1D | 1E | 1F | | 7 | 8 |
| 20 | 21 | 22 | 23 | | 8 | 9 |
| 24 | 25 | 26 | 27 | | 9 | 10 |
| 28 | 29 | 2A | 2B | | A | 11 |
| 2C | 2D | 2E | 2F | | B | 12 |
| 30 | 31 | 32 | 33 | | C | 13 |
| . | . | . | . | | . | . |
| . | . | . | . | | . | . |
| . | . | . | . | | . | . |
| 3F0 | 3F1 | 3F2 | 3F3 | | FC | 253 |
| 3F4 | 3F5 | 3F6 | 3F7 | | FD | 254 |
| 3F8 | 3F9 | 3FA | 3FB | | FE | 255 |
| 3FC | 3FD | 3FE | 3FF | | FF | 256 |

| 8 | 8 | 8 | 1 |
|---|---|---|---|
| NO. OF BITS | | | |
| AU | AL | DATA | R/W |
| DATA IN ADDRESS | | | |

Figure 7.4 Record Buffer Organization

MPA address, FFFE is mapped into OFFE and address FFFF is mapped into OFFF. The content of these addresses are called the restart vector, because they determine where the first instruction is read from when the MPA is initialized. In the MPA, the first instruction is stored in location 800.

#### 7.2.2.4 Peripherals

The 6800 is designed such that all peripherals appear as memory locations. The MPA is designed such that certain addresses (in the range of 2000 and above) are assigned to peripherals.

##### 7.2.2.4.1 Control Panel

The control panel appears as memory location 2000 to the MPU. The switches on the control panel that the 6800 senses are organized as nine groups of 8-bit words. The 6800 writes nine data words into eight latches located on the control panel. Each data word is decoded on the panel and is used to drive a group of switches. The outputs of all the switches are ORed together and applied to the data bus when memory address 2000 is read.

The decoding of the data bus into drive signals (SMD1 through SMD9) for the control panel switches is shown in Figure 7.5. The encoding of the switch outputs into 8-bit words is shown in Figure 7.6.

##### 7.2.2.4.2 Record Processor

Figure 7.7 is a tabulation of the memory addresses and the meaning of the data associated with each address that is used for information exchange between the MPU and the Record Processor.

The MPU monitors the status of the Record Processor by reading location 2001.

When the MPU determines that the Record Processor is armed, it:

1. Stops reading the control panel switches.

2. Outputs the Start Event (2 bytes) and Stop Event (2 bytes) by writing in locations 2007, 2009, 200B, and 200D.

3. Outputs a byte ( only 4 bits are used) of control information by writing in location 2003.

4. Outputs a second byte of control information by writing in location 2005.

Writing in location 2005 is interpreted by the Record Processor as a command to begin searching for a start event.

| SMD - | DATA BUS INPUT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 4 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 5 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 6 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 7 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

Figure 7.5 Data Bus Decoding of Address 2000

```
SMD1 - START PAGE
SMD2 - START ADDRESS
SMD4 - STOP PAGE                    - HEX SWITCHES
SMD5 - STOP ADDRESS
SMD7 - DISPLAY SELECT PAGE


BITS:  7 6 5 4 3 2 1 0

SMD3 - X H N   R   E F   START EVENT
         L-R W-/-R V-X   QUALIFIERS
         T M   W   T T
                         (X= NO SWITCH)
BITS:  7 6 5 4 3 2 1 0

SMD6 - X X   R   E E E   STOP EVENT
           W-/-R V-O-X   QUALIFIERS
             W   T S T

BITS:  7 6 5 4 3 2 1 0

SMD8 - S N S N L S P M   MISC.
       G-R C-R S-E-G-E
       L M T M T O E M   FUNCTIONS

BITS:  7 6 5 4 3 2 1 0

SMD9 - X D M A L U D R   MORE
         M-P-L F-P-W-G   MISC.
         A U L T   N T   STUFF
```

Figure 7.6 Switch Encoding

MPU - RECORD PROCESSOR DATA EXCHANGE:

| LOCATION AND TYPE | BIT: 7654 3210 | DESCRIPTION | MNEMONIC |
|---|---|---|---|
| READ $2001 | XX1X<br>X1XX<br>1XXX | RP ARMED BIT<br>BUFFER FULL BIT<br>VALID DATA IN RPB BIT | |
| WRITE $2003 | 1XXX<br>0XXX<br>XX11<br>XX01<br>XX10<br>X1XX<br>X0XX | NORM (VS. HALT) RECORD MODE<br>HALT (VS. NORM) MODE<br>RECORD ALL ACCESSES<br>RECORD MPU ACCESSES ONLY<br>RECORD DMA ACCESSES ONLY<br>EOS STOP EVENT<br>EXTERNAL OR EVENT STOP<br>(SEE BIT 2, WRITE $2005) | NOSTP<br>STPOEV<br>RECAL<br>RECMP<br>RECDM<br>EOSTP |
| WRITE $2005 | 1XXX 0XXX<br>0XXX 1XXX<br>X001 X001<br>X010 X010<br>X011 X011<br>X1XX X1XX<br>X0XX X0XX<br>START STOP<br>ONLY ONLY | SINGLE INSTRUCTION GO MSG<br>NORMAL GO MESSAGE<br>READ ACCESS FOR EVENT<br>WRITE ACCESS FOR EVENT<br>READ OR WRITE ACC FOR EVENT<br>EXTERNAL INPUT<br>EVENT INPUT (HEX SWITCHES) | SIGO<br>NORGO<br><br>STAWQ STPWQ<br>STAEWR STPEWR<br>MPSTA MPSTP<br>- - |
| READ $2003 | XXXX XXXX | ADDRESS COUNTER OF REC PROC | |
| WRITE<br>$2007<br>$2009<br>$200B<br>$200D<br>$200F<br>$200F | XXXX XXXX<br>XXXX XXXX<br>XXXX XXXX<br>XXXX XXXX<br>XXXX XXXX<br>XXXX XXXX | START EVENT MOST SIG BYTE<br>" " LEAST SIG BYTE<br>STOP " MOST " "<br>" " LEAST " "<br>RP ARM RESET ENABLE | |

Figure 7.7 MPU - Record Processor Data Exchange

### 7.2.3 Block Diagram Description

This section describes the functions of each of the PCB assemblies in terms of block diagrams.

#### 7.2.3.1 MPU

The MPU PCB block diagram is shown in Figure 7.8. The arrows on the data and address buses indicate which parts of the buses are unidirectional and which are bidirectional.

The oscillator frequency is 22.008 MHz (Block 1), which is divided by 5 X 6 = 30 (Block 2) to give a 733.6 KHz (T = 1.363 µsec) clock for the 6800. The CRT clock frequency is 22.008 ÷ 5 = 4.4016 MHz. Block 3 consists of 7400 gates that decode the phase one and phase two clocks and clock drivers that use discrete NPN and PNP transistors to generate the proper two-phase clock levels required by the 6800.

The Direct Memory Access Request line ($\overline{DMAR}$) is clocked by a flip-flop so that it is presented to the 6800 at the required time (Block 4).

Block 5 consists of two flip-flops that debounce the Clear switch ($\overline{CLR}$) and generate a clear pulse when either the Clear switch is activated or the power is turned on.

Blocks 6, 7, 8, and 9 are bus drivers that are mechanized using 74126 tri-state buffers. Block 9 is bidirectional, whereas blocks 6, 7, and 8 are undirectional.

Block 10 decodes the address bus and generates the enable signals that are used to control the tri-state drivers and to select RAM or ROM.

Block 11 consists of ten 7407s that are required to ensure that the minimum "1" level driving the address lines of the ROMs are 3.0 V or greater.

Block 12 consists of two 2708 (1024 X 8) ROMs and one 2704 (512 X 8) ROM.

Block 13 consists of eight 2102 (1024 X 8) static RAM devices.

A read/write (R/W) flip-flop and drivers for driving the RAM and the system R/W line are also located on the MPU PCB

Block 14 is the 40-pin 6800 MPU.

#### 7.2.3.2 CRT Driver

Figure 7.9 is a block diagram of the CRT Driver PCB. The CRT Driver performs three basic functions:

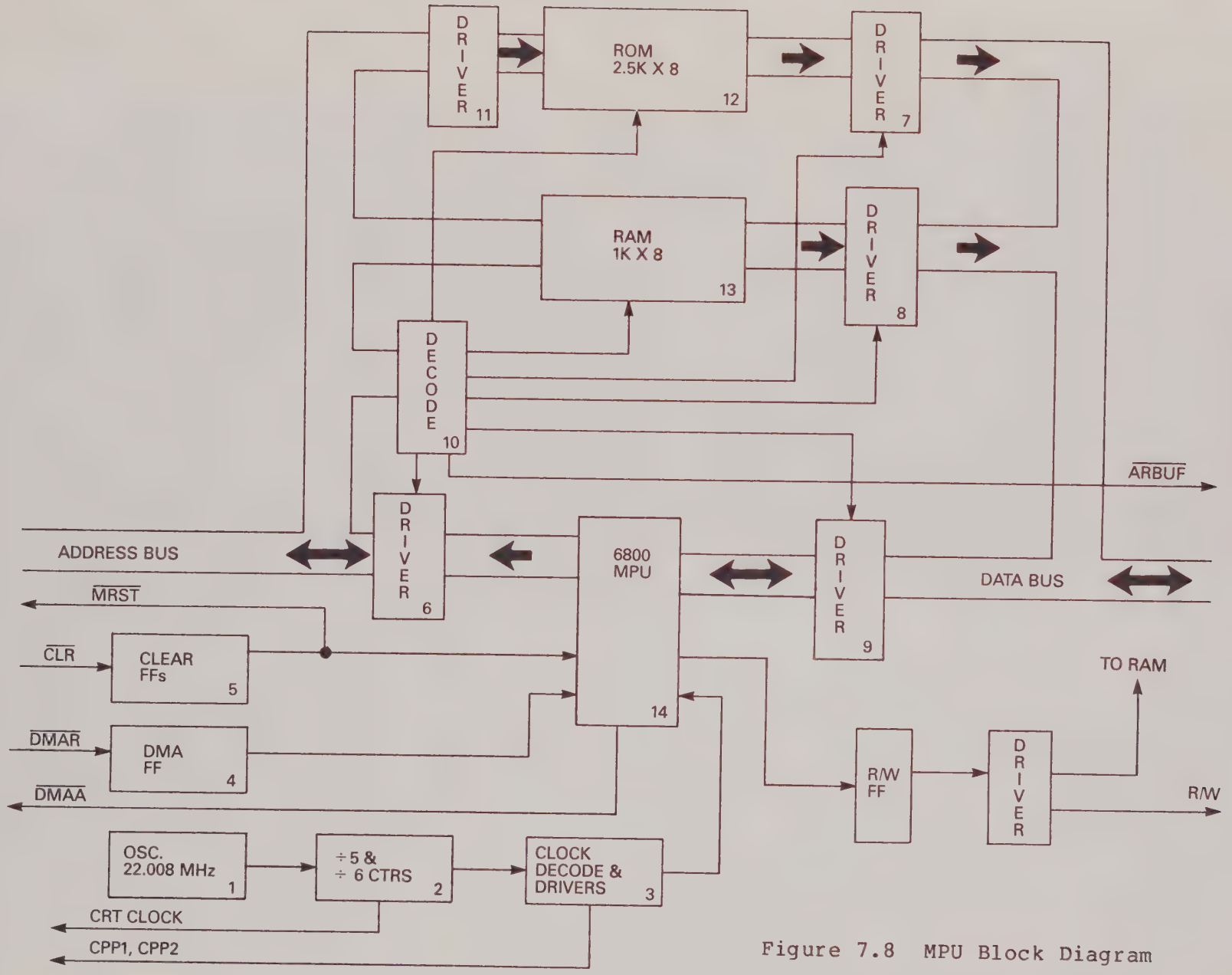



Figure 7.8 MPU Block Diagram

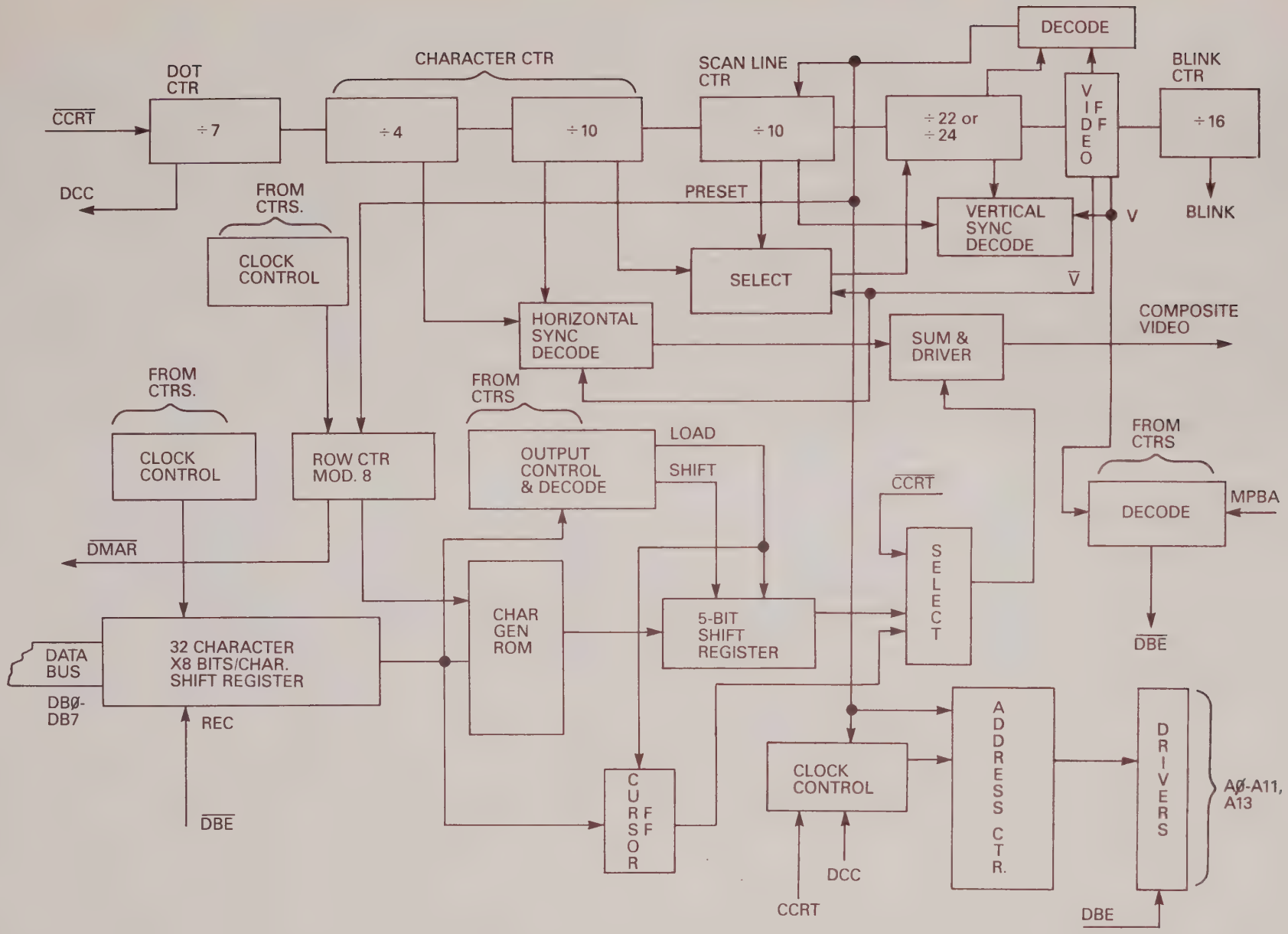



Figure 7.9 CRT Driver Block Diagram

1. Counts down the CRT clock (CCRT) in such a way as to generate the signals required for the other two functions and to generate the vertical and horizontal synchronization pulses and combine them with the video.

2. Loads the 32 character line buffer from the proper locations in RAM at the proper times.

3. Recirculates the data in the line buffer, driving the character generator ROM, and generating the video signal that is combined with the vertical and horizontal synchronization signals to form a composite video signal.

7.2.3.2.1 Countdown Chain

The countdown chain consists of six counters (74161s), two flip-flops, and several gates. The counters operate synchronously, counting down the CCRT clock pulses (F = 4.4016 MHz, T≈227 nsec) to generate a horizontal sync pulse frequency of $4.4016 \times 10^6 \div 7 \times 4 \times 10 = 15,720$ Hz. This is further counted down in groups of ten scan lines to give 240 scan lines during the display time. An additional 22 scan lines are counted for the vertical retrace time, which occurs every 240 + 22 = 262 scan lines or at a frequency of 15,720 Hz ÷ 262 = 60 Hz. This is further divided by 16 to obtain a signal with which to blink characters or the cursor 3.75 times each second.

Sixteen equalizing horizontal sync pulses are given to the monitor after the vertical sync pulse and before data is displayed (this time is called vertical scan delay).

The raster scan sequence is as follows:

| Vertical | Time in Scan Lines |
|---|---|
| sync delay | 3 |
| sync pulse | 3 |
| scan delay | 16 |
| Total | 22 scan lines |

| Horizontal | Time in Characters |
|---|---|
| scan delay | 3 |
| video | 32 |
| sync delay | 2 |
| sync pulse | 3 |
| Total | 40 character times |

The total number of scan lines is:

22 + 24 X 40 = 262 lines.

7.2.3.2.2 Data Manipulation

This consists of loading the lines of data from RAM, recirculating them, and simultaneously applying the data to a ROM character generator, reading the dots for the characters out, loading them in parallel into a 5-bit shift register, and shifting them out serially at the proper time.

7.2.3.3 Record Data

Figure 7.10 is a block diagram of the Record Data PCB. The card performs the following functions:

1. Holds the record buffer in which the data is recorded.

2. Holds the start and stop event addresses in latches.

3. Compares the start and stop events with the address lines from the SUD.

4. Holds the address counter that points to the record buffer.

5. Holds the delay counter.

6. Decodes the addresses used for the control of the Record Processor.

7. Holds the multiplexers and bus drivers that enable the MPU to read the address counter, the record buffer, and the status of the record processor.

8. Provides a path for signals that flow between the SUD and the record control PCB.

7.2.3.3.1 Record Buffer Operation

The record buffer is mechanized using 25 256 X 1 static RAMs. During recording (RECBF true), the chip selects of all of the RAMs are held low and when the record clock ($\overline{\text{RECW}}$) goes low, data is written into all 25 RAMs. The address counter (two 74S161s) is reset to zero before recording begins and is incremented using the record clock. The address counter (8 lines) is selected by two 74157 quad two-to-one multiplexers as the address lines to the record buffer during recording. After recording, the RAMs are selected in three groups of eight and one group of one when the MPU reads the record buffer. The multiplexer selects the MPU address bus as the address lines to the record buffer when the MPA is not recording.

7.2.3.3.2 Compare Operation

The stop event (16 bits) and start event (16 bits)

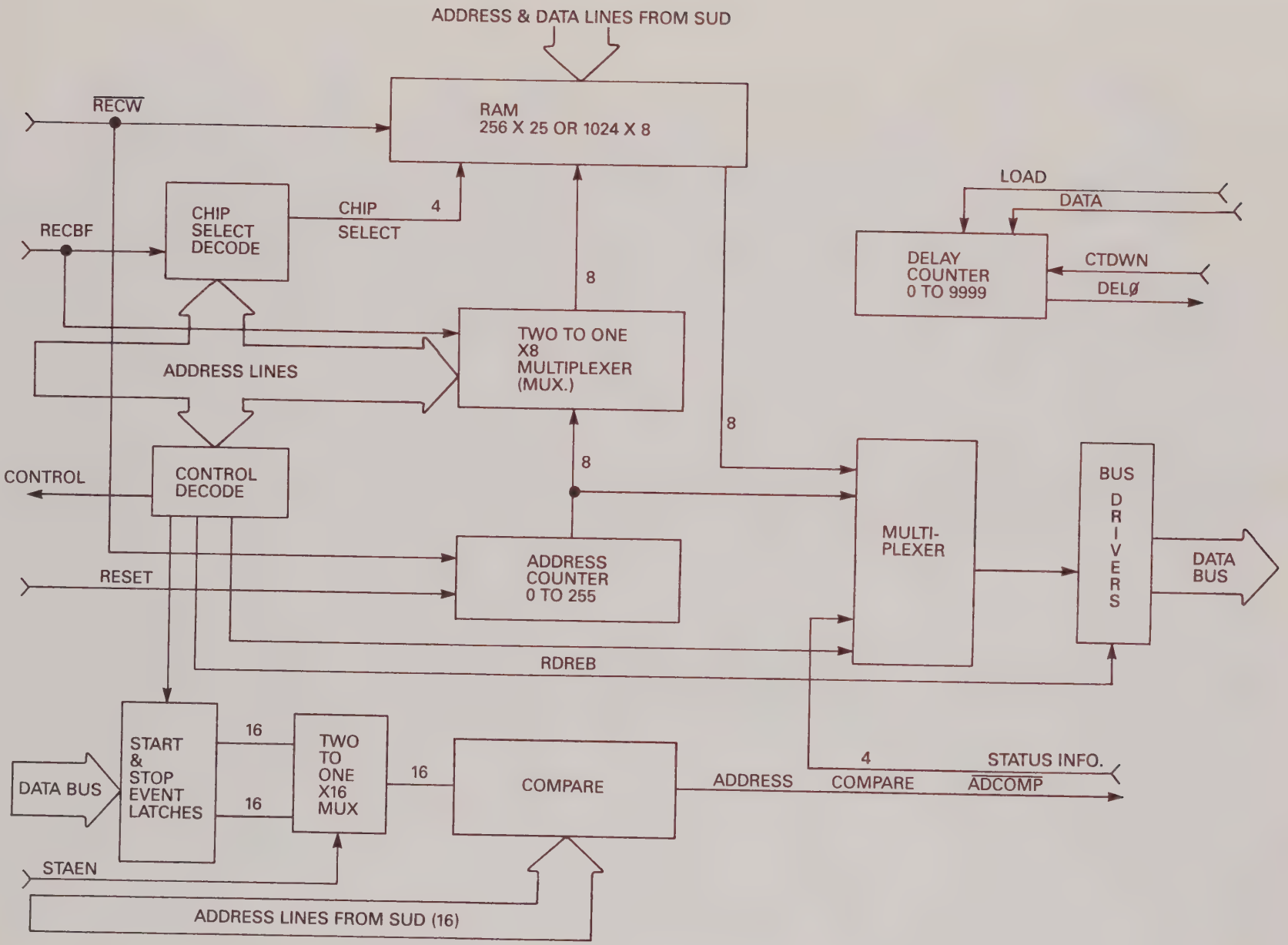



Figure 7.10 Record Data Block Diagram

are loaded into latches prior to recording. After arming the MPA, the signal STAEN selects the start event to be compared with the address lines of the SUD. After the start event is found, STAEN goes low and the stop event latches are compared with the SUD address lines.

7.2.3.3.3 Delay Countdown

The delay counter consists of four 74192 BCD counters. When the MPA is either cleared or armed, the delay digitswitches are read by the record processor and their value loaded into the delay counter. The counter is then counted down using a signal equivalent to the record clock until it is equal to zero.

7.2.3.4 Record Control

Figure 7.11 is a block diagram of the Record Control PCB. As the name implies, the card consists of logic that controls the recording of information in the record buffer.

Block 1 consists of three 74LS175 quad latches that the MPU loads with control information.

Block 2 consists of five flip-flops and several gates. The function of block 2 is to debounce the arm switch, generate a single pulse, generate a "GO" signal, and generate a reset signal.

After being reset or armed, the delay switches are sampled and loaded into the delay counter. The logic that controls this is a 74161 counter and a 7442 decoder (shown as block 3).

The address compare is further qualified in block 4. A flip-flop (called the Start/Stop FF) determines whether the search is for the start or the stop event. When the start event is found the flip-flop is set and the next compare is the stop event.

Block 5 contains the start event latch, the stop event latch, the record flip-flop, and logic that controls when and under what conditions the preceding are set and reset.

The clocks from the microprocessor in the SUD are regenerated in a form suitable for using to record the data in block 6. Different clocks are selected depending upon what microprocessor is in the SUD.

Depending upon the position of the delay modifier switch and the value of the delay switches, the clocks occurring between start and stop events are used either for recording or for decrementing the delay counter. This is done in blocks 7 and 8.

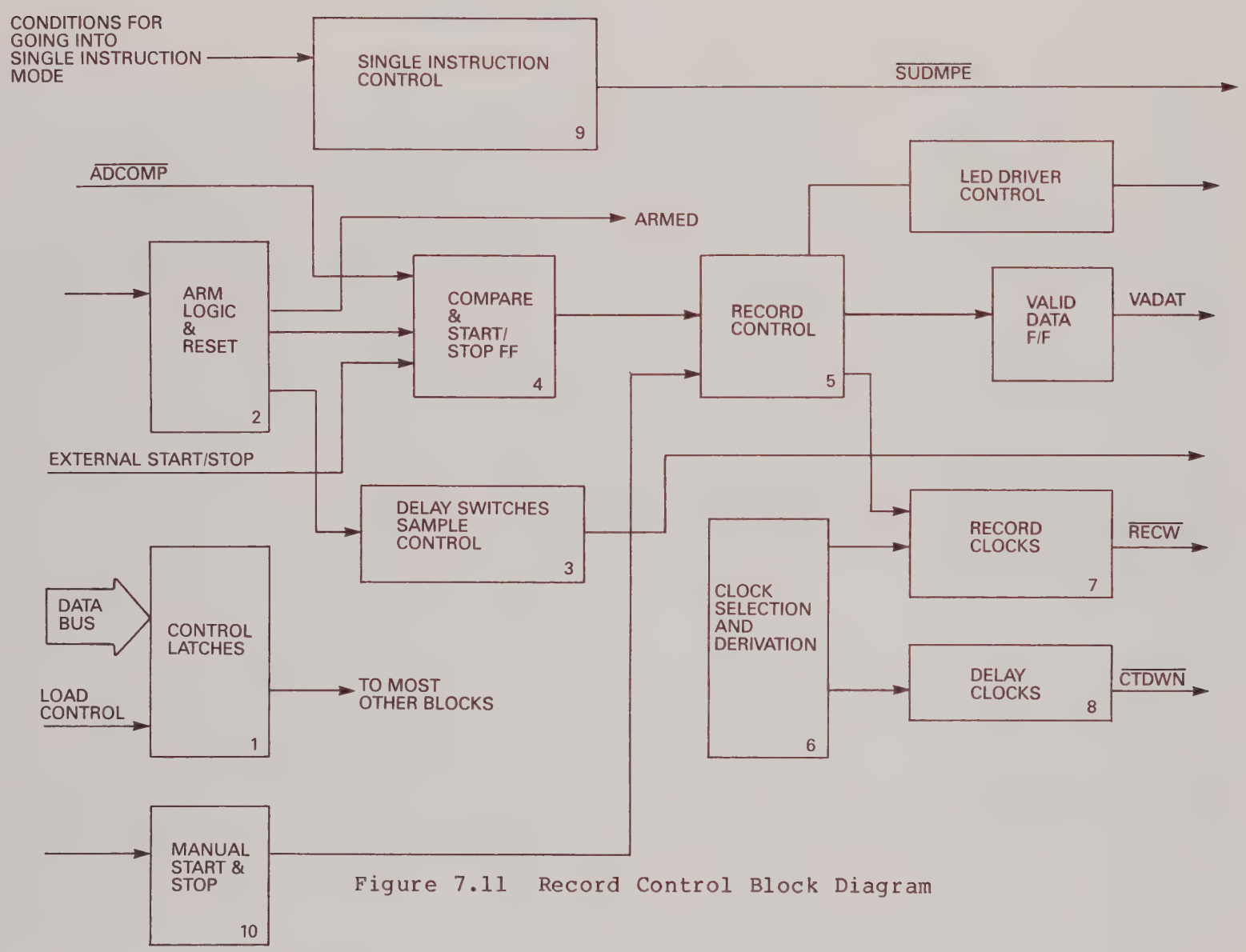



Figure 7.11 Record Control Block Diagram

Block 9 contains the logic that controls, (1) the single instruction execution operating mode, and (2) going from normal to single and vice versa.

Block 10 debounces the Manual Start /Stop switch.

7.2.3.5 Control Panel

A block diagram of the control panel is shown in Figure 7.12. For purposes of explanation the control panel is divided into three areas - A, B, and C.

7.2.3.5.1 Section A; Digital MPU

This section consists of all of the switches except the Delay, Delay Modifier, Arm, Clear, Power On, and Manual Start/Stop switches. The 6800 MPU scans all of the other switches by writing different data into eight latches and reading the positions of the switches. The outputs of all of these switches are "ORed" together using diodes at the inputs to the data bus drivers. Reading from location 2000 enables the data bus drivers.

7.2.3.5.2 Section B; Analog

This section consists of the source followers for the external start, stop, and arm inputs, the analog comparators, and the threshold selection and adjustment switches and pot.

7.2.3.5.3 Section C; Miscellaneous

The delay switches are read by the record processor. the LEDs are driven by signals from the record control PCB. The Arm and Manual Start/Stop switches go to the record control PCB and the start, stop, and delayed start/stop signals come from the record control PCB and go to the output BNCs.

7.2.3.6 Personality Module

The personality modules for the 6800 and 8080 MPUs are so simple that no block diagrams are presented. The reader is referred to the schematic diagrams in Section IX. Schematics for other personality modules will not be a part of this manual but will be supplied with each personality module.

7.2.4 Operating Modes

The MPA has two basic operating modes - Normal and Single Step. In the Normal mode, the MPA is transparent to the MPU in the SUD. In the Single Step mode, the MPU in the SUD is controlled by the MPA. Each time the Single Step switch is activated, the MPU executes one instruction and then goes into a "wait state".

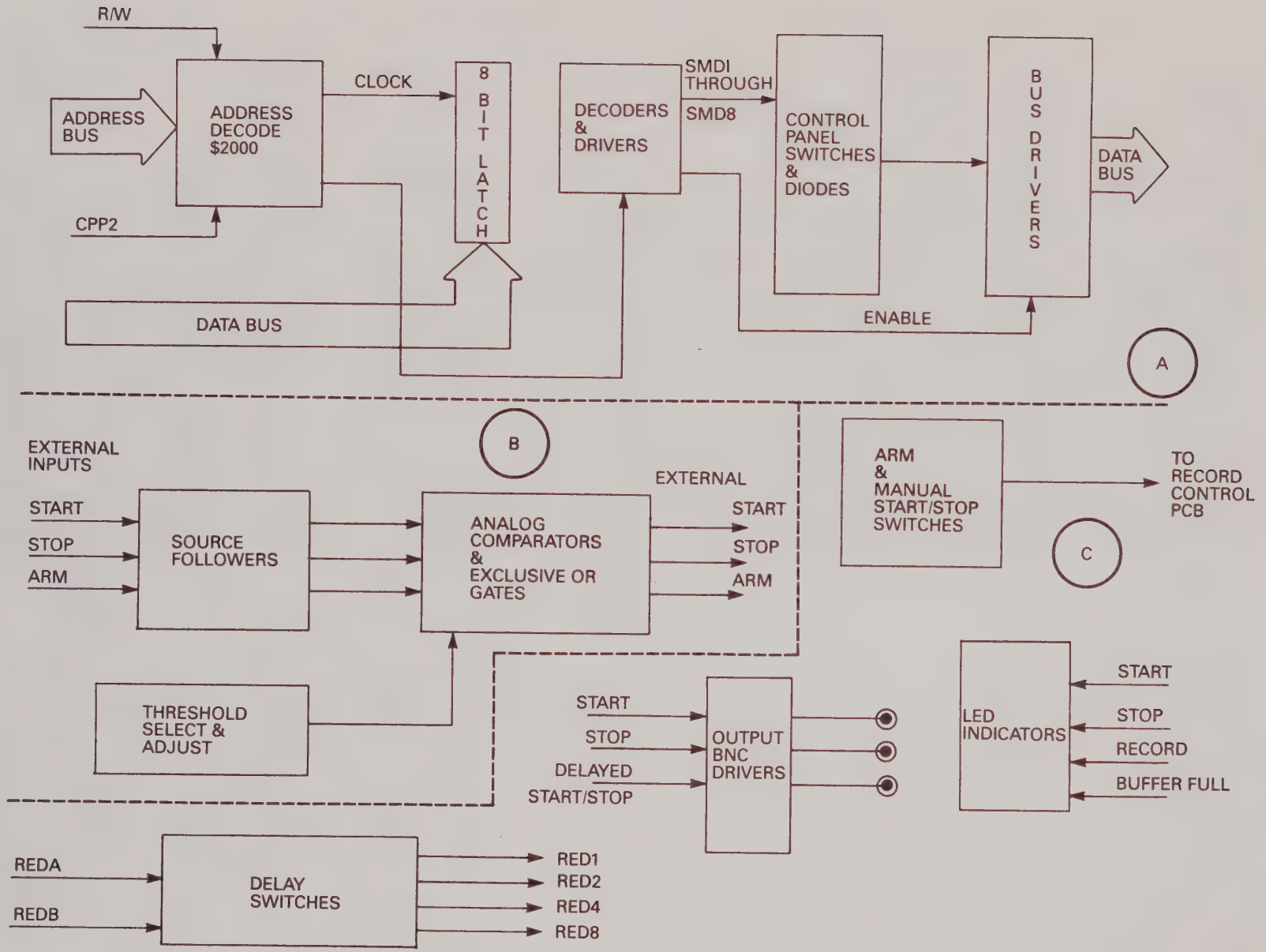



Figure 7.12 Control Panel Block Diagram

#### 7.2.4.1 Changing Modes

The MPA goes from normal to single when the Record Select switch is in the HALT position and the stop event occurs. If there is delay applied to the stop event, it is timed out before the MPU in the SUD is halted.

The MPA can also go from single to normal and then back to single. This is useful for quickly going through a long loop or to "continue" to a second breakpoint that is many instructions away from the instruction at which the SUD was halted.

#### 7.2.4.2 Loop Count

When the Record Select switch is in the HALT position and the Arm switch is in the AUTO position, certain flip-flops on the record control PCB are not reset after a record operation. This was done so that if the stop event is an access in a loop, the stop event BNC outputs a pulse every time the program goes through the loop. If an event counter is connected to the stop event BNC, it reads (totalize) the number of times the program goes through the loop.

What the MPA does in this case is to halt the MPU in the SUD and allow the MPU in the MPA to update the display before rearming and searching for another stop event. Because the MPU in the SUD is halted while the display is updated, the program in the SUD is executed at less than real time. The operator can see the execution by observing the activity in the memory or page display modes.

#### 7.2.4.3 MPU - Record Processor Interaction Simplified

Figure 7.13 shows the interaction between the MPU and the record processor at a macro-operation level. The operations performed by the MPU are on the left and the operations peformed by the record processor are on the right. Interaction between the two is indicated by a broken line.

The MPU is usually in a section of the program called an "idle loop." It scans the control panel, responding to operator requests for new data display formats, updating of cursor data, and testing for an armed condition. Testing for the armed condition is actually a part of the idle loop, but is shown separately for clarity.

When the MPU reads bit 5 of address 2001 as a "one," it knows that the instrument wants to be armed and acts accordingly. The one is a result of (1) the arm switch being put in either auto or manual or (2) an external arm input when the arm switch is in the external position. In either case, the MPU responds by taking the most recent front panel data, formatting it, and writing it in the record processor control and data latches. The writing of

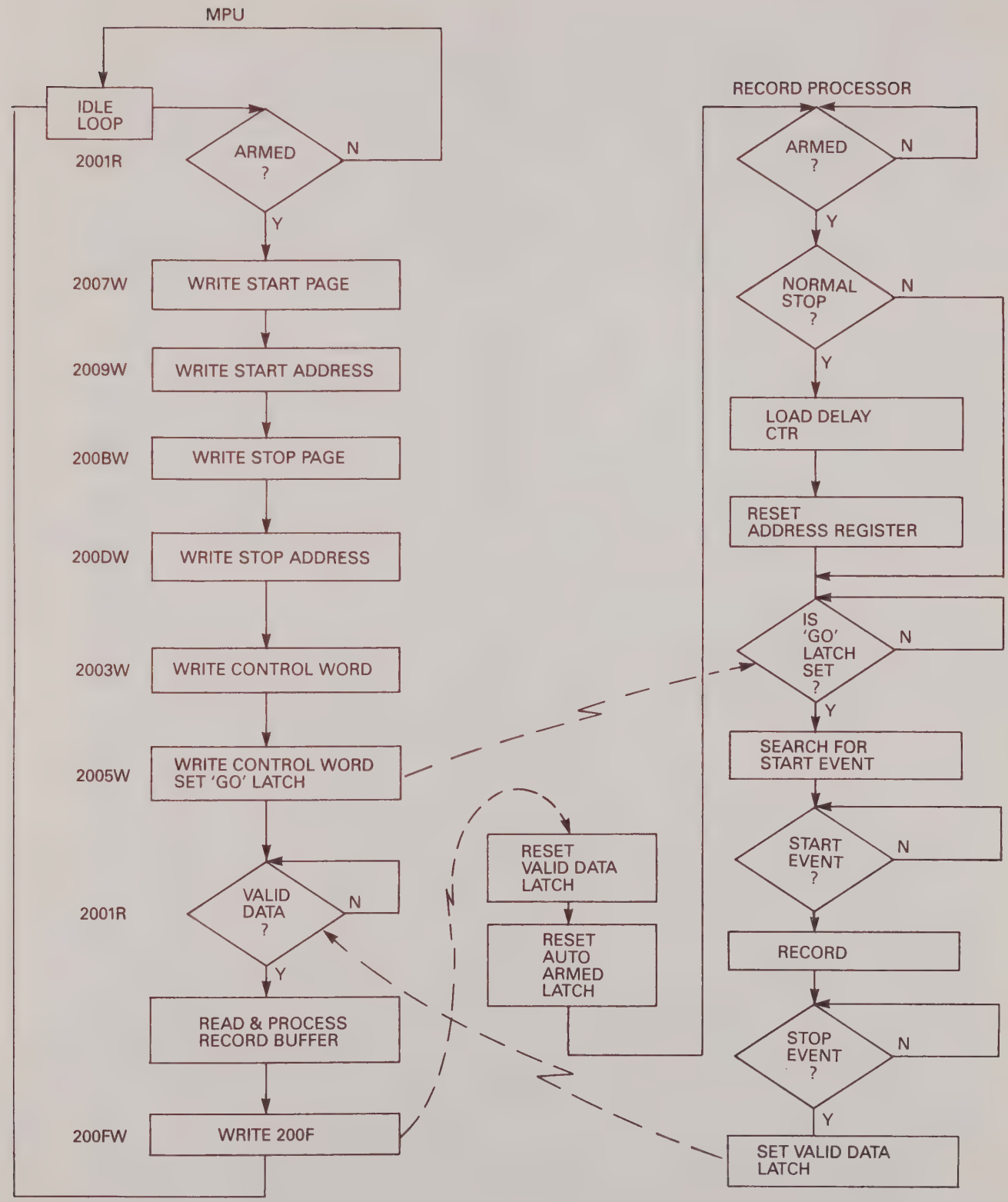



Figure 7.13 MPU - Record Processor Simplified Interaction Flow Chart

the second control word (2005W) sets the "Go" latch, which causes the record processor to search for a start event. After setting the Go latch, the MPU waits for the valid data flag from the record processor. The record processor performs the recording operation and sets the valid data latch when it is finished. The MPU then reads the data in the record buffer, updates the display, and writes in 200F, which tells the record processor that it (the MPU) is finished. The MPU then goes back to its idle loop. Meanwhile, writing in location 200F resets the valid data latch and the auto armed latch, which reinitializes the record processor.

## 7.3 Detailed Description

### 7.3.1 MPU PCB (see Figures 9.8 and 9.9)

#### 7.3.1.1 Power on Reset

The R3 C6 RC time constant provides 300 ms of delay when power is turned on or when the clear switch is released. Debouncing is accomplished by clocking the clear signal through a D flip-flop using a signal (pin 32; scope sync) that occurs once each frame time (T = 16.67 ms).

#### 7.3.1.2 Oscillator and Clock Divider

The 22.008 MHz oscillator is divided by 5 by the 74161 when forced to count from 11 to 15. The terminal count is used to preset the counter to count 11. Counts 14 and 15 (BC) are decoded for the CRT clock (CCRT, pin 98), giving a 4.4016 MHz waveform with a 2/5 or 40% duty cycle. The second 74161 is clocked using $\overline{B \cdot C}$. It divides by 6, counting from 9 to 14. The phase one clock to the MPU is decoded as $\overline{BC}$ and the phase two clock as C. The relationship between the CRT clock and the MPU phase one (CPP1) and phase two (CPP2) clocks are shown in Figure 7.14.

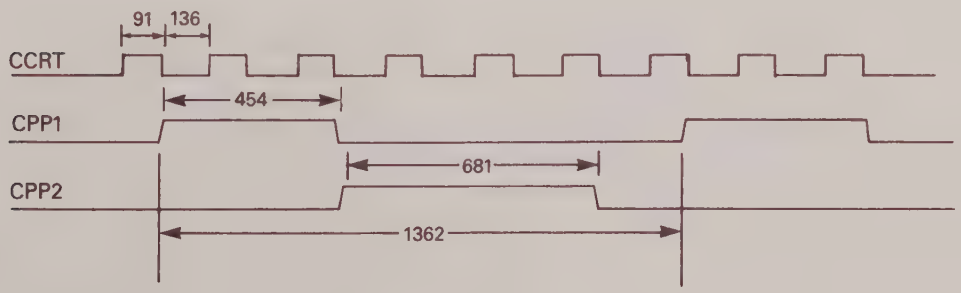



Figure 7.14 CRT - MPU Clock Relationship

### 7.3.1.3 Address Decoding

The address lines from the MPU are decoded to generate the enables for the RAMs, ROMs, and their associated buffers. When power is turned on or when the clear switch is activated, the MPU places FFFE on the address bus and expects to read the upper byte of the address where the first instruction is located. The MPU then outputs FFFF and expects to read the lower byte of the address where the first instruction is located. In the MPA, the restart vector is located in address OFFE. The address transformation is:

FFFE becomes OFFE,
FFFF becomes OFFF.

This is done by decoding the MPA lines A15 through A12 to 1s and using it to change the corresponding address lines to the memory to all 1s. This is done by the 7442 on the MPU PCB. The four inputs are:

A = A10
B = A11
C = A12 $(\overline{A14} + \overline{A15})$
D = A13 $(\overline{A14} + \overline{A15})$

The 7442 is used as a one of eight decoder with the D input being low to enable the outputs. When A13 = 1 and A12 = 0, peripherals are addressed so the decoder is disabled.

The binary weight of A10 is $2^{10}$ or $1024_{10}$. Thus the decoder selects memory to 1K (1024) resolution.

### 7.3.1.4 Bus Enable

The address and data bus drivers must be enabled at the proper times. The data bus is bidirectional.

The address bus enable is:

$$MOABE = \overline{BA}\left[APAGE + A13 + ARBUF\ \overline{RECORD} + AROM\right].$$

This says that the MPU output bus is enabled unless the processor is halted ($\overline{BA}$) and when addressing the 2102 RAM (APAGE) peripherals (A13), the record buffer (ARBUF), or program memory (AROM).

The MPA input data bus enable is:

$$MPIDBE = READ \cdot MOABE.$$

The MPA output data bus enable is:

$$MODBE = (WRITE + BA)\ APAGE + WRITE\ \overline{BA}\ (A13 + ARBUF\ \overline{RECORD})$$

The signal $\overline{RECORD}$ is always true.

The bus enable for reading from the page RAM is:

$$PRDBE = READ \cdot APAGE + BA.$$

The BA signal allows the RAM to be read by the CRT driver card when MPU is halted.

7.3.1.5 EROM BUFFERS

The address and chip enable inputs to the 2704 and 2708 EROMs require a minimum of 3.0 V for a logic 1. Because the minimum 1 output of TTL is 2.4 V, 7407 buffers with pullup resistors to 5 V are used.

The EROMs are specified to sink the current from one TTL load (1.6 mA). Other loads (CRT, Control Panel, Record Control, Record Data) are on the data bus. Although EROM is not read to these loads and some are outputs and not inputs, buffers are provided. The buffer enable is reading EROM (AROM).

7.3.2 CRT PCB (see Figures 9.6 and 9.7)

7.3.2.1 Countdown Chain

The $\overline{CCRT}$ signal is counted down by six 74161 counters and two flip-flops operating synchronously at 4.4016 MHz.

The technique employed is to use the terminal count of each stage to preset that stage to a count P, equal to the full modulus of the counter (16) less the number of counts (N) that are desired (P = 16 - N). This is illustrated by Figure 7.15, which can be used to verify to what count the counter should be preset in order to divide by a given number of clocks.

| DIVIDE BY | COUNTER OUTPUTS D C B A | PRESET TO |
|---|---|---|
| 16 | 0 0 0 0 | 0 |
| 15 | 0 0 0 1 | 1 |
| 14 | 0 0 1 0 | 2 |
| 13 | 0 0 1 1 | 3 |
| 12 | 0 1 0 0 | 4 |
| 11 | 0 1 0 1 | 5 |
| 10 | 0 1 1 0 | 6 |
| 9 | 0 1 1 1 | 7 |
| 8 | 1 0 0 0 | 8 |
| 7 | 1 0 0 1 | 9 |
| 6 | 1 0 1 0 | 10 |
| 5 | 1 0 1 1 | 11 |
| 4 | 1 1 0 0 | 12 |
| 3 | 1 1 0 1 | 13 |
| 2 | 1 1 1 0 | 14 |
| 1 | 1 1 1 1 | 15 |

Figure 7.15 Preset of 74161s

7.3.2.1.1 Frame Counter

The raster scan sequence is as shown in paragraph 7.2.3.2.1. The actual counting sequence of the frame counter is shown in Figure 7.16. The X column represents the Q output (pin 6) of the 74109 flip-flop in location A10. A, B, C, and D are the outputs of the 74161 counter in location B10. The display time is signified by the video flip-flop (A10 pin 10) being true. During this time the data is painted on the face of the CRT and the frame counter is enabled every tenth scan line. At the end of the display time the counter is preset to 5 and the vertical blanking interval begins. During this time, the frame counter is enabled every scan line. at the end of the vertical blanking interval the frame counter is preset to 4, the scan line counter is preset to 6, and the cycle is repeated.

The blink counter (74161 in C9) is enabled once per frame (each 16.67 msec). Its output is used to gate on and off the video for the cursor and any other blinking characters.

7.3.2.1.2 Character Counter

The character counter consists of two 74161 counters in positions A7 and A8. It is enabled with the terminal count of the dot counter, which occurs once each character time (1.589 µsec). The character counter counts modulo 40 (4 X 10) as there are 40 character times per scan line. The counting sequence and the decoding for the horizontal sync pulse are shown in Figure 7.17. Each time the character counter reaches its terminal count the scan line counter is enabled.

7.3.2.1.3 Dot Counter

The dot counter divides the CRT clock by 7. The horizontal portion of each character consists of five dot times, with two dot times between characters to give seven dot times per character block.

7.3.2.2 Character Generation and Data Manipulation

7.3.2.2.1 Character Display Format

The character block is shown in Figure 7.18. As previously explained, a display line consists of ten scan lines. The first scan line is always blank. This is the time during which a display line of 32 characters is read from RAM and loaded into a 32 bit X 8 shift register. During scan lines 2 through 10, the data is recirculated and the dots are painted on the screen. Scan line 9 is always blank and scan line 10 may or may not be blank depending upon whether or not there is a cursor associated with that

FRAME COUNTER OUTPUTS

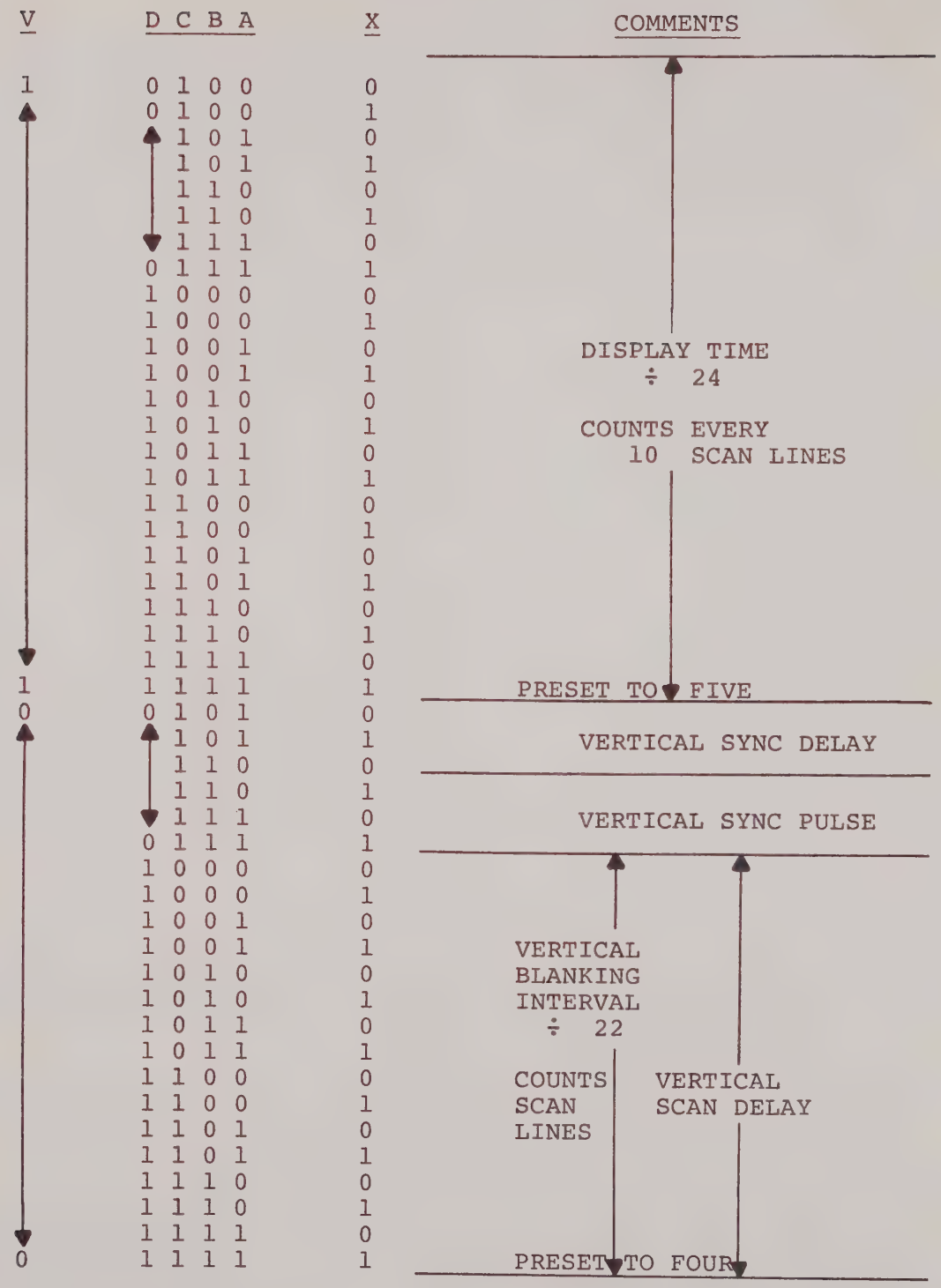



Figure 7.16 Raster Scan Count Sequence

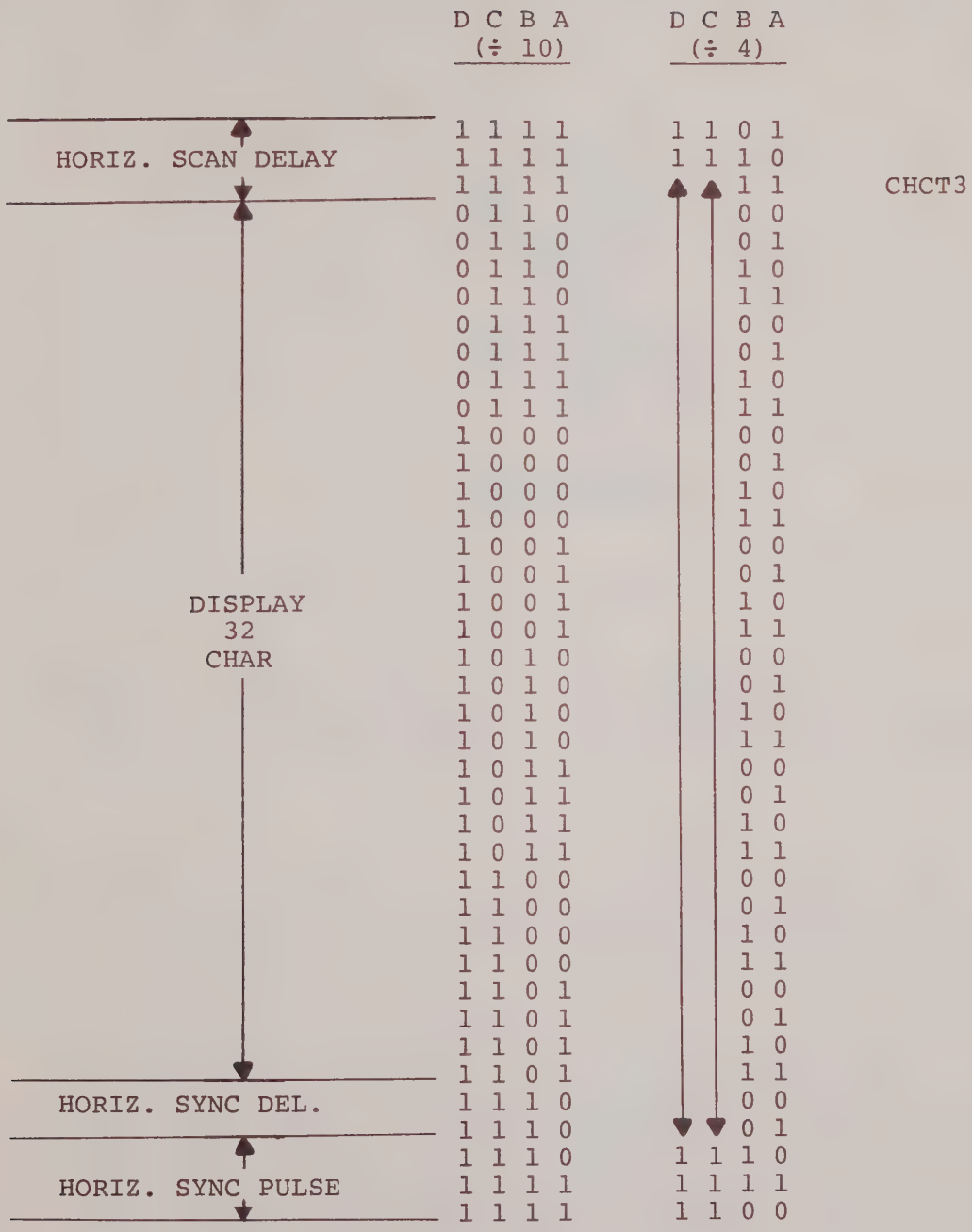



Figure 7.17 Character Counter Count Sequence

particular character. In the horizontal direction there are two dot times between characters. In the vertical direction there are three scan lines between rows of characters, with the cursor occupying the middle line.

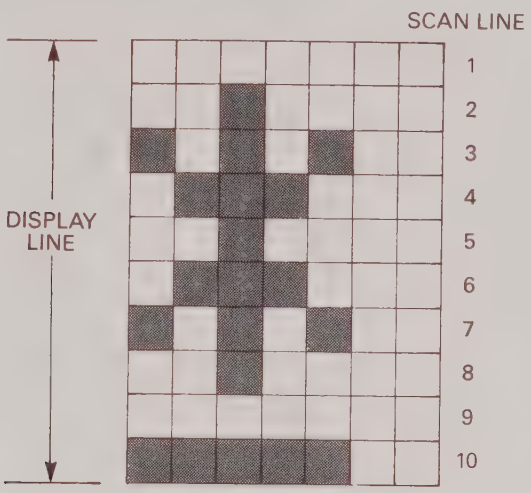



Figure 7.18 Character Block (7 X 10)

The representation of the character in Figure 7.18 is not completely accurate because the data is anded with $\overline{CCRT}$ to give a 60% duty cycle for the dots. The cursor is not anded with the clock so it appears brighter and as a continuous line (not a series of dots).

7.3.2.2.2 Loading a Line of Data

When the video flip-flop is low (A10 pin 10) and the frame counter reaches its terminal count (B10-15 high), the frame counter is preset to 4, the scan line counter is preset to 6, the address counter is preset to $100_{16}$, and the row counter is preset to 8. The $\overline{DMAR}$ line (pin 91) goes low, requesting control of RAM from the MPU. When the video flip-flop is set, the scan line counter reaches count 1 (SL1 = 1), and the MPA relinquishes control of RAM (MPBA = 1, pin 89). $\overline{DBE}$ goes low (B5 pin 6) when the $\overline{BCD}$ goes high and the address counter outputs (D5, D6, D7) are applied to the address bus. The dot counter C output (DCC) is used as the clock for loading and recirculating the line buffer. The equation for the line buffer clock is:

$$LBCP = DCC \left[ DBE + \overline{BCDD} \cdot ASL \right].$$

When loading the line buffer (DCC • DBE) the signal $\overline{BCD}$ is used (part of DBE) to enable the clock. After 32 clocks the first character is at the last (output) position in the buffer. However, when displaying the data (ASL) the clock must not occur until after the data is displayed so the $\overline{BCD}$

signal is delayed one character time ($\overline{BCDD}$). The data bus enable ($\overline{DBE}$) signal is used directly to control the recirculate input to the line buffer. The same clock (DCC) is used to advance the address counter as is used to shift the line buffer when loading it.

7.3.2.2.3 Character Generation

After the line buffer is loaded (SL1), it is recirculated for nine scan lines (SL2 through SL10). Data is displayed during active scan lines, ASL = 1 (all except SL1 and SL9). The data from the line buffer is applied to the character generator ROM in parallel (6 bits for the 64 displayable ASCII upper case characters). The upper two bits (DB6 and DB7) are used to designate the cursor and blinking characters, respectively. The cursor bit is used to disable the character generator, whose outputs are three state and are pulled up to $V_{CC}$ with resistors. When the video shift register is loaded (PEVSR), all ones are entered if the cursor bit is a one because the character generator is disabled.

After shifting the data out of the video shift register, the register contains all zeros. If the parallel entry pulse is disabled all zeros are shifted out. This is the technique used to blink characters.

The output of the video shift register is anded with $\overline{CCRT}$ for all characters except the cursor. This causes all characters to be composed of dots as opposed to lines when the X component of a character is greater in length than one dot time.

The row counter counts modulo 8 (8 to 15) and selects which row (of 5 bits) is read in parallel from the character generator. The clock to the row counter (CPRCT) occurs just prior to displaying the first character (CHCT3). It is asymmetrical because it occurs only during scan lines 3 through 8, inclusive.

7.3.2.3 Composite Video

The horizontal and vertical sync pulses and the video are added together to form a composite video signal and sent to the CRT monitor. Transistor Q1 functions as a video adder and emitter follower, generating a 1.5 V peak-to-peak composite video signal as shown in Appendix A, Figure A-1. The periods of the horizontal and vertical sync pulses are as shown in Appendix A. The width of the horizontal sync pulse is three character times or 3 X 1.589 μsec = 4.767 usec, and the width of the vertical sync pulse is three scan lines or 3 X 63.56 μsec = 190 μsec.

7.3.3 Record Data PCB

For logic diagram, refer to Figure 9.11. The functions

of the record control card are explained in paragraph 7.2.3.3

7.3.3.1 Record Buffer

The record buffer consists of 25 27LS01 type (256 X 1) RAMS. When recording, the chip selects of all 25 RAMs are low (pins 3, 4, 5) and the address counter (C5, C8) outputs are selected by the multiplexers (C4, C7) and applied to the RAMs. The address counter is reset to zero when the MPA is either cleared or armed and is incremented with the positive edge (after recording) of the record clock ($\overline{\text{RECW}}$).

The data inputs to the RAM (pin 13) are the inverse of the SUD address bus, data bus, and read/write line. The outputs of the RAM (pin 6) is the inverse of the input so the data appears in its true form.

When the MPU reads the record buffer (RECBF = 0), the MPU address bus lines are decoded according to Figure 7.4 by D6, D11, C1, and by applying A2 through A9 to the address line multiplexers (C4, C7). The chip enables (C3) select one of four groups of bytes and the other address lines select the word (1 of 256 bytes). When reading the contents of the buffer RDRB is true (selecting the buffer C6, C10) and RDREB is true enabling the data bus drivers to put the contents of the record buffer on the MPU data bus.

7.3.3.2 Control Decode

Gates D5, D6, D9 and decoder D10 are used to decode the MPU address bus, to generate the signals used to load the control latches on the record control PCB, the start and stop event latches on the record data PCB, and to enable the output multiplexers (C9, C6, C10) and the data bus drivers (C11, C12).

When $\overline{\text{2001R}}$ is low the MPU is reading the status flags from the record control PCB. When $\overline{\text{2001R}}$ is high RDRB selects either the record buffer (RDRB = 1) or the address counter RDRB = 0).

The start and stop events are loaded into latches by $\overline{\text{2007W}}$, $\overline{\text{2009W}}$, $\overline{\text{200BW}}$, and $\overline{\text{200DW}}$. These signals are generated when the MPU writes into these addresses.

7.3.3.3 Address Compare

Either the start event (STAEN = 1) or the stop event (STAEN = 0) is selected by multiplexers (B14, B15, B16, B17) for comparison with the SUD address bus. Actually, the inverted signals are compared. If a pair of address lines compare, there is a low level on the anode of the respective diode (CR1 through CR16). If all sixteen address lines compare, there is a low on the cathode of all sixteen diodes ($\overline{\text{ADCOMP}}$ = 0).

7.3.3.4 Delay Counter

The delay counter consists of four 74192 BCD counters (D1 through D4). It is preset when the MPA is either cleared or armed and counts down a signal called CTDWN. When it reaches count zero (DELO = 1), the clocks are inhibited and the counter stops counting.

7.3.4 Record Control PCB (see Figure 9.13 for logic diagram)

As previously explained in paragraph 7.2.3.4, the record control card controls the recording of information in the record buffer. This operation is shown in the five blocks of Figure 7.13 beginning with "search for start event" and ending with "set valid data latch". The recording operation is described in terms of the control flip-flops and latches on the record control PCB in Figure 7.19.

7.3.4.1 Record Operation

7.3.4.1.1 Arming the MPA

The MPA can be armed in three ways; manually, automatically, or externally, depending upon the position of the ARM switch (15) on the front panel (Figure 4.1).

When S15 is in the MANUAL position, a low is present on pin 20 ($\overline{\text{ARMM}}$) of the record control PCB. The switch is debounced by clocking it with $\overline{\text{SCPSYN}}$ into a D flip-flop (D4). The signal is then synchronized to the MPA by clocking it into a second flip-flop (C4), which is also used to generate a reset pulse (D3-8) and to set the Armed latch (C4 pin 5 = 1).

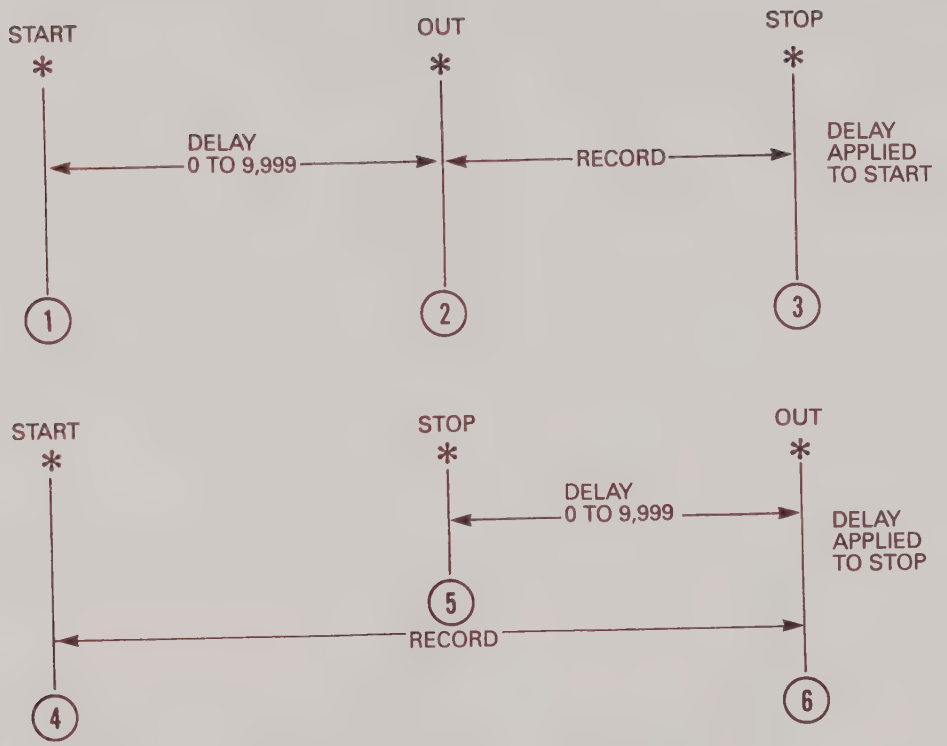
When S15 is in the AUTO position, a low is present on pin 19 ($\overline{\text{ARMA}}$) of the record control PCB. The Armed latch is set as explained in the preceding paragraph.

When S15 is in the EXTERNAL position and if the input from the ARM BNC (24) exceeds the selected threshold, pin 23 (EXARM) is high. The Armed latch is set as before. Setting the Armed latch causes the start event search LED (1) to go ON (pin 17, STASH = 1).

The MPU, which has been reading 2001, detects that the record processor is armed and sends the required control words to it. Writing the last control word ($\overline{\text{2005W}}$ = 0) and being Armed causes a "Go" condition (A2 pin 6 = 0).

7.3.4.1.2 Searching for a Start Event

The GO condition (B11 pin 3 = 0) enables the start event latch (B12-4, 5, 6 and B11-1, 2, 13, 12) to be set




1 Reset start event search flag.
2 Delay = 0, set stop event search flag, set Record FF. Output on delay BNC.
3 Reset stop event search flag, reset Record FF, set valid data FF. Output STOP BNC.
4 Reset start event search flag, set stop event search flag, set Record FF.
5 Reset stop event search flag. Output on STOP BNC.
6 Delay = 0, reset Record FF, output on delay BNC.

Figure 7.19 Recording Operation

when a start event occurs. When the MPA is armed, the start flip-flop is reset (A14 pin 5 = 0) and the Start Event Search LED is ON, indicating that the MPA is searching for a start event ($\overline{STAOT}$ = 0).

The start event can be either a memory access or an external input. If it is a memory access it is further qualified by being a read, a write (STAWQ = 1) or either a read or a write (STAERW = 1). This comparison is made by gates B8-8, 9, 10; C14-8, 9, 10; B9-1, 2, 13, 12; C11-9, 10, 11, 8 and A13; D10-9, 10, 8; and D6-5, 6. Three ones are required at the pin 9, 10, and 11 inputs to C11 to get a compare (C11-8 = 0).

If the start event is an external input the compare is performed by turning on transistor Q1. Gates A5-3, 4, 5, 6 and A7-13, 11 and D flip-flop B7-2, 3, 5 are used. Note that the outputs of the start flip-flop are used to select whether the comparison is being made on the start or the stop events.

The comparison is performed during the positive duration of the SUD phase two clock (SUDCP 2 = 1). If a compare occurs, the start event latch is set (B12-4 = 0, B11-12 = 1); if the delay applies to the stop event (DELSTP = 1, A12-6) the Record flip-flop is set and recording begins. If the delay applies to the start event (DELSTA = 1, A9-11) the Record flip-flop is not set until the delay counter reaches zero (DELO = 1, A9-10). In the latter case, the delay counter counts down the signal CTDWN pin 75 until DELO = 1 and then recording begins.

7.3.4.1.3 Recording

7.3.4.1.3.1 Record Clock Generation

The compare is peformed for the entire positive duration of the SUD phase two clock. The clock that is used for recording ($\overline{RECW}$) is determined by whether an 8080 type SUD or a 6800 type SUD is connected to the MPA.

For 8080 type SUDs, the signal SUD1C (pin 33) is low. If the record status switch in the 8080 personality module is ON (SWSTAT = 1), the status is recorded using SYNC and the entire positive duration of the SUD phase one clock (gate C10-3, 4, 5, 6). Instruction fetches and input instructions are recorded by using DBIN and the entire positive duration of the phase two clock (gate C10-9, 10, 11, 8). Output instructions and memory write operations are recorded using the fact that $\overline{SUDR}$ is high ($\overline{WR}$ = 0 on 8080) and the entire positive duration of the phase two clock (gate C10-1, 2, 13, 12).

For 6800 type SUDs a short clock is generated from the rising edge of the phase two clock when SUDVMA is true.

This is shown in Figures 5.3 and 5.4. The gates that are used are D12-1, 2, 3, 4, 5, 6, 8, 9, and C11-1, 12, 13, 12. The DMA clock operates in a similar manner using D13-1, 2, 3, and C12 and C11-3, 4, 5, 6.

The countdown clock (CTDWN, pin 75) is either the record clock (RECW) if the delay is not zero and applies to the stop event or (when not recording) an equivalent clock if the delay is not zero and applies to the start event and the MPA is in normal (as opposed to single step).

7.3.4.1.3.2 Setting and Resetting the Record Flip-Flop (FF)

The Record FF is asynchronously set (A11 pin 4) and synchronously reset using the record clock. When the Record FF is set (A11 pin 5 = 1), record clocks are generated and applied as write strobes to the record buffer RAMs. The Record FF is set when the Start Event latch is set, the delay counter is equal to zero, and the delay applies to the start event (DELSTA = 1) or when the Start Event occurs (STARTE = 1) and the delay applies to the Stop Event (DELSTP = 1). The Record FF can also be set by placing the Manual Start/Stop Switch (16) in the START position.

The Record FF is reset when any one of the following conditions occurs:

1. The Manual Start/Stop Switch is in the STOP position (MPSTPR = 1, A10 pin 1).

2. The record buffer is full (EOS = 1) and the Stop Event is EOS (EOSTP = 1, A9 pins 2, 13).

3. The Stop Event occurs and the delay applied to the Stop Event and it is a normal Stop Event (NOSTP = 1).

4. The delay is timed out and the delay applied to the Stop Event and the Stop Event Latch is set.

When the Record FF is reset its $\overline{Q}$ output going high is used to set the Valid Data FF, which tells the MPU that the record buffer contains valid data.

The Record FF is not reset when the Record Control Switch (14) is in the HALT position and a Stop Event occurs. Under these conditions the MPA allows the MPU in the SUD to complete the execution of the current instruction before it causes it to halt. This is accomplished by resetting (C6 pin 1) the Normal/Single (NS) FF.

7.3.4.1.4 Mode Changing

The MPA can go from Normal to Single and then from Single to Normal (back) to Single.

7.3.4.1.4.1 Normal to Single

When going from Normal to Single the following events occur:

1. The Stop Event is detected.

2. The NS FF is reset.

3. The Stop Event Latch is not reset (unlike the normal record operation).

4. A second flip-flop called the Single Sample (SS) FF is set (B2 pin 5 = 1). This flip-flop controls the $\overline{\text{SUDMPE}}$ line, which in turn controls the Ready (or $\overline{\text{Halt}}$) line of the MPU of the SUD.

When SS FF is set, and if the MPU of the SUD is a 6800 type MPU (SUD1C = 1), counter B1 is enabled. It counts sixteen SUDCP2 clocks, reaches its terminal count and causes the SS FF to be reset and the Valid Data FF to be set. Counting these clocks ensures that the MPA has a sufficient number of clocks to complete the recording of the current instruction.

The 8080 sends a one on bit 5 of its data bus at SYNC time to indicate an instruction fetch. This signal (SUDESI) is used to reset the NS FF and set the Valid Data (VD) FF.

7.3.4.1.4.2 Single Stepping

Resetting the NS FF, the SS FF, and the Single Cycle (SC) FF (B3 pin 5 = 0) causes three ones to be applied to A4 pins 9, 10, and 11, which cause its output (pin 8) to go low. This signal is inverted (D5-3, 12) and applied to the enable input of a 74126 three-state bus driver (whose input is grounded) in the personality module. This causes the MPU in the SUD to go into a "wait" or "pause" state.

When the operator depresses the single step switch (13) the MPU in the MPA detects it and loads the appropriate control words. In this case a single instruction go ($\overline{\text{SIGO}}$ = 0) control message is sent. This causes a clock at B3 pin 12, which causes the flip-flop to be set. The SC FF is then set when the next SUDCP1 clock occurs. The SC FF goes true from one SUDCP1 to the next SUDCP1 and causes the SS FF to be set. The SC FF causes $\overline{\text{SUDMPE}}$ to be pulsed low for 6800 type SUDs, which allows the MPU to execute one instruction. For 8080 type SUDs, the SS FF causes $\overline{\text{SUDMPE}}$ to go low until SUDESI goes true.

The process described in the preceding paragraph is repeated whenever S13 is in the SINGLE position. The pause and repeat operation is a function of the program.

7.3.4.1.4.3 Single to Normal to Single

This operation may also be called a "continue". A different Stop Event can be entered, S13 depressed (so MPU reads new stop Event), and S13 put in the Normal position. The MPA then allows the MPU in the SUD to advance to the new Stop Event (or breakpoint) and then halts the SUD MPU.

To do this, the MPU in the MPA sends a "normal go" message (NORGO 0), which resets the Stop Event latch so that the record logic searches for a Stop Event. The conditions now are the same as going from Normal to Single and the operation is, therefore, identical.

7.3.4.2 Counting Loop Iterations

When S14 is in the HALT position and the MPA is in Auto Arm (S15 in AUTO), the MPA halts the MPU in the SUD, updates the display, and rearms itself and searches for a new Stop Event. If the Stop Event is an access in a loop, each time the access occurs a pulse occurs on the Stop Event ouput BNC (30). An event counter can then be used to count the number of times the program goes through the loop. This is accomplished by not presetting the NS FF if S14 is in the HALT position. A side effect is that to initialize the MPA, S14 must be in the NORMAL position and the clear switch (S34) must be activated twice; once to load the latches and once to generate the clear pulse (RESCONI = 0). Furthermore, if the operator then wants to halt the MPU in the SUD, S14 must be put in the HALT position and the clear switch activated again.

7.3.5 Control Panel PCB

Refer to the Schematic Diagram in Section IX.

7.3.5.1 Digital MPU Section

This section includes all the switches scanned by the MPU. Writing in address 2000 is decoded and ANDED with the phase two clock to generate a pulse to sample the data bus into eight latches. The outputs of the latches are decoded according to Figure 7.5 and ANDED with the phase two clock and the condition that the MPU is peforming a read operation. This signal is also used to enable the data bus drivers.

The SMD signals are generated by turning on a particular emitter follower transistor. When the emitter follower is off, looking into the emitter is essentially an open circuit. The diodes are required on the outputs of the hexadecimal switches to isolate the common (SMD line) from each other. For the same reason, diodes are required on the common contacts of the other switches. The outputs of all

of the switches are connected together in groups of eight (labeled 0 through 7) and connected to the respective data bus driver input. When the emitter follower is off, the 470 resistors pull the bus driver inputs to a low level so that the MPU reads a zero on the data bus.

7.3.5.2 Analog Section

The three external BNC inputs (Start, Stop, Arm) are connected to dual FET, zero offset buffer amplifiers, which drive 521 comparators. The comparator output for the External Arm input goes directly to the record control PCB. The External Start and External Stop comparator outputs are compared as to slope using exclusive OR gates before the signal is sent to the record control PCB.

Diode clamping is used to limit the FET gate voltage to $\pm$5.5 V. Zero offset is achieved by using dual FETs and biasing the one used as a load on and forcing the same current to flow from the -12 V supply as from the +12 V supply through precision (1% tolerance) resistors.

The ten turn 1 KΩ pot (R27) can adjust the variable threshold from +3 V to -3 V. The TTL X1 position selects 2 V as the reference and the TTL X10 position selects 0.2 V as the reference.

7.3.5.3 Delay Switches

The same technique is used to read the delay switches as is used to read the hexadecimal switches. The REDA and REDB signals are from a 74161 counter on the record control PCB. The data is loaded in parallel, 4 bits at a time, into four 74192 BCD counters on the record data PCB.

7.3.5.4 Indicators

Open collector (7405) inverters are used to forward bias the status LEDs, which turn them ON.

7.3.6 Personality Modules

The schematics for the 8080 and 6800 personality modules are included in Section IX (Figures 9.19 and 9.17).

7.3.7 Motherboard

The interconnection list for the motherboard is included in Section IX (Figure 9.15). The RF choke is used to keep RFI generated by the +12 V to 9.5 kV voltage converter in the CRT monitor from affecting the logic.

# SECTION VIII

# MAINTENANCE

## 8.1 Introduction

This section covers maintenance and disassembly procedures for troubleshooting and repair of the Model 168-D Microprocessor Analyzer. System analysis is performed with the aid of a diagnostic procedure for the Front Panel controls and functions.

To facilitate the diagnostic procedure, special test programs contained in C2704 ROMs (Front Panel program and RAM program) are used in conjunction with special PCB configurations in the 168-D. Details on these special tests are mentioned in their respective sections.

Because Biomation uses separately purchased CRT and Power Supply sections in the 168-D, the diagnostic procedure does not cover them. As an addition to this manual, the manufacturers manual on their respective subassemblies are contained in Appendices B and C. An explanation on mnemonic usage is presented in Appendix E.

A PC board exchange program was set up with the factory for use by customers within the continental United States, with regional service centers in foreign countries. In addition, waveform photographs have been included with the schematics to aid service personnel who wish to troubleshoot to the component level. Additional assistance in a particular problem can be obtained by contacting the Customer Service department at the factory: Phone (408) 255-9500 TWX 910 338 0226.

In summary, there are three methods of service available:

1. Return the entire unit to the factory or service center for repair.

2. Trace the problem to the defective PC board and obtain a replacement board from the factory or service center.

3. Troubleshoot the problem to the component level with the aid of the diagnostic procedure and schematics or with the aid of factory personnel.

## 8.2 Test Equipment and Test Aids

See Section 6.2 for the necessary items to conduct the

diagnostic procedure for the 168-D. The following should also be available:

1. Model 851-D Digital Logic Recorder.
2. 8080 SUD.
3. ROM 2704 (Front Panel program).
4. ROM 2704 (RAM program).

## 8.3 Control Panel Diagnostic

Before continuing this part of the diagnostic procedure, review the Standard Handling Precautions of RAM, ROM, and MPU devices found in Appendix D.

Remove the 168-D top cover. Review this section for the disassembly procedure. Remove the bar that blocks removal of the PCBs. Remove the MPU PCB. Install the Front Panel program in ROM location C1. See Section IX for PCB locations. Remove the Record Control and Record Data PCBs from their mother board sockets. It is not necessary to remove the RC and RD PCBs completely from the chassis. Lift them up enough for complete disconnection from the system. Place the MPU board back into its respective slot and socket. Position the controls on the panel as shown in Table 8.1. Switch on the AC power and wait approximately two minutes for the system to warm up. Observe the screen and verify that the presentation compares to that in Figure 8.1A. The Front Panel program scans all the switches on the Front Panel except the AC Power, Clear, Threshold, Start, Stop, Delayed Start/Stop Memory Cycle, Start/Stop, Manual, and Arm switches. These switches and their functions are covered in later portions of the diagnostic procedure.

Observe the 168-D screen and switch the Start Event Source switch to EXT. Verify that the cursor moves under the EXT term. Check the remaining switches in the same manner. The Thumbwheel switches should have corresponding readings with those on the screen.

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| Cursor not moving under term as directed by Front Panel switch position. | Observe the screen and verify which term(s) fails the diagnostic test. Refer to Figure 7.6. Determine which SMD is failing from the switch list. Locate the respective SMD on the front panel schematic diagram. SMD1, 2, 4, and 5 should have a waveform at the "C" input of the HEX/DEC |

Table 8.1 Control Panel Settings

| | | | |
|---|---|---|---|
| START EVENT | | | |
| Source | Ext | Event | |
| Mode | Read | R/W | Write |
| Page-Address | 0 0 | 0 0 | |
| STOP EVENT | | | |
| Source | Ext | EOS | Event |
| Mode | Read | R/W | Write |
| Page-Address | 0 0 | 0 0 | |
| DISPLAY SELECT | | | |
| Normal/Select | Norm | Std | Select |
| | Mem | Page | Seq List |
| Page | 0 0 | | |
| DELAYED START/STOP EVENT | | | |
| Memory Cycles | 0 0 0 0 | | |
| | Start | Stop | |
| RECORD MODE | Norm | Halt | |
| | Norm | Std | Single |
| ACCESS | All | up | DMA |
| MANUAL | Start | Std | Stop |
| ARM | Auto | Ext | Manual |
| CURSOR | Neutral | | |
| THRESHOLD | X1 | Var | X10 |
| START SLOPE | + | - | |
| STOP SLOPE | + | - | |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
| --- | --- |
| | switches as depicted in Figure 9.5, photo 2. This waveform is typical of the "C" inputs when no digits are switched in. Figure 9.5, photo 3, represents the "C" input when a digit is switched in. This same figure represents the waveform present at SMD 3, 6, 8, and 9. The high level inputs to the anodes as directed by the various switch positions are high level outputs to the data bus. Using a scope, observe which SMD is failing and determine if the signal is getting passed the diode. If not, determine if the signal is getting to the diode. If not, check U9 or U10 (CA3082). Check the HEX/DEC switches if the Start Event and/or Stop Event digits fail. |
| Cursor appears under some but not all of the terms. | Check the outputs of U2 and U1 depending upon under what term the cursor is missing. |
| Cursor appears under every term and FFFF appears in the Start/ Stop Event codes. | Check the input to U13-4. Pin 4 should have high level pulses. |
| Turn the 168-D off. Replace the Front Panel program with the 0C00 programmed ROM. Connect all PCBs. Place the 168-D in the Analytical mode using a 6800 SUD and personality module. Adjust the frequency generator for a triangle waveform at 5 kHz and 8 V p-p. Using a BNC-T adaptor, connect the signal output to CH 2 of the scope and to the ARM input on the 168-D. Set the Front Panel switches as follows: | |

| | |
| --- | --- |
| Start Event Source | Event |
| Start Event Mode | R/W |
| Start Event | 0C23 |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| Stop Event Source — Event<br>Stop Event Mode — Read<br>Stop Event — 0C30<br>Stop Event Delay — 0000<br>Stop Event Arm — EXT<br>Stop Event Threshold — Variable | |
| With the 6800 SUD, 6800 PM, and function generator connected to the MPA, turn on the MPA and SUD. Verify that data at memory accesses 5, 10, and 13 are decremented as the MPA is armed and recording. | |
| With the ARM switch in EXT the system does not arm using the external 5 kHz signal. | Check the external arm circuit on the Front Panel PCB. The EXT ARM signal comes from U16-4. See Figure 9.5, photo 1. If the squarewave signal is not presented at J10-6, check the input to Q3-2.<br><br>Check the output of C5 on the Record Control PCB. |

## 8.4 System Clear Diagnostic

Connect the 168-D to the 6800 SUD and personality module. The SUD should have a Shift program installed. Set the Front Panel switches as follows:

Start Event Source — Event
Start Event Mode — Read
Start Event Page — 0C
Start Event Address — 00

Delay — 0000
Delay Modifier — Start

Stop Event Source — Event
Stop Event Mode — Read
Stop Event Page — 0C
Stop Event Address — 10

Record Select — Normal
Record Control — Normal

Display Select — MEM

Access — µP
AC Power — OFF (down)

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| Turn on the AC power to the system. Observe that the screen is blank initially. Wait approximately two minutes. The fixed fields for the Memory Display mode will appear. No data should appear in the variable fields. See Figure 8.1B. | |
| System initializes with data in the fixed fields. System won't clear. | Check $\overline{\text{POR}}$ circuit on the MPU PCB, composed of K4-6, C9, B9 and associated circuitry. Check B9-3 for the scope sync input (CLK). |

## 8.5 Normal (passive) Record Operation Diagnostic

| | |
|---|---|
| Manually Arm the MPA by moving the Arm switch to the manual position. The Start Event Search LED will go on. | |
| Start Event Search LED does not come on. | Check D5-8 on the Record Control PCB. Pin 8 should go high. If it does but the SES LED stays off, check U14-12 on the Front Panel PCB. If U14-12 goes low, the LED CR1 is bad or VCC is not present, which should be evident by not having the red LED (AC) come on when power is applied.<br><br>If C4-5 does not go high with manual arm, check the $\overline{\text{ARMM}}$ input to D4-12 and the associated circuitry. See Figure 9.13, photo 1, for the CPP1 Clock. See Figure 9.13, photo 2, for the $\overline{\text{SCPSYN}}$ clock.<br><br>If the $\overline{\text{ARMM}}$ input does not go low when the ARM switch is activated, check the front panel S19 (ARM). |
| Reset the SUD. Observe the following on the CRT (see Figure 8.1C): | |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| 1. Cursor located at Page 00.<br>2. Access (*) at Page 01.<br>3. Access (blinking *) at Page 0C.<br>4. Total accesses of 19.<br>5. (Blank) to cursor.<br>6. (Blank) at cursor.<br>7. * to left of start.<br>8. * to left of stop.<br>9. Blanks in cursor data fields.<br>10. Start field: 0C 00 8E R.<br>11. Stop field: 0C 10 8C R. | |
| CRT reflects other than described data in Figure 8.1C. | Check cable connections for intermittent connection. Review the Front Panel switch positions. Clear the MPA. Manually arm. Reset the SUD and observe displayed data again. |
| Cursor not located at Page 00. | Cursor location is based on a subroutine in the software program. Initialization and screen displays are a function of Front Panel switch positions.<br><br>Check ROM C1 (0C00). |
| Access (*) not at Page 01. | Check the Record Buffer on the Record Data PCB. Check ROM C1 (MPU PCB). The Access at Page 01 reflects a W (write) access. |
| Access not blinking at Page 0C. | Check ROM C1. The blinking (*) indicates a stop access and should reflect the same page as the Stop Event qualifier. |
| Total accesses less or more than 19. | If less than 19 the system is detecting a Stop Event different than the programmed Stop Event. Check cable connections, ROM (Shift program in SUD), and the MPU in the personality module. |
| Blank to or at cursor containing data. | To Cursor defines the position of the cursor in the MPA |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
| --- | --- |
| | memory. If the cursor is positioned under an access, it should reflect where that access is in the MPA memory. If To Cursor is not blank but the cursor is a 00 on the CRT, check ROM C1.<br><br>At Cursor defines the total number of accesses on the programmed page. Because the cursor initializes at Page 00, this space should also be blank. If it is not blank and the cursor is in the correct position on the CRT, the error suggests a software fault. Check ROM C1. |
| Asterisks not present to the left of Start/Stop. | The asterisk to the left of start said that the Start Event was the same as programmed on the Front Panel. Check the Delayed Start/Stop Event Thumbwheel switch and Start/Stop switch. Check the Start Event compare circuits on the Record Data PCB (D15, 14, 13 and 12, and B17 and 16).<br><br>The asterisk to the left of the Stop Event represents the same function as the Start Event. If the asterisk is missing, the SUD stop address is not comparing to the Front Panel switch data. Check the Stop Event compare circuits C16, 15, 14, and 13, and B15 and 14. |
| Start Field other than shown. | Check Start Event Thumbwheel switches. Check associated circuits on the Record Data PCB. Check Record Buffer RAM. Check ROM C1. |
| Stop field other than shown. | Review above; same as Stop Event. |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| 8.6 Cursor Movement Diagnostic | |
| Move the cursor one position to the right. See Figure 8.1D. Observe that the data in the cursor data field is:<br><br>Page 01 Address 00 Data 00 Type W<br><br>Observe that there are 11 accesses to the cursor. | |
| Cursor stays in the same position. | Review the Front Panel diagnostic. Check ROM C1. |
| 8.7 Page Mode (RAM Page) Diagnostic | |
| Select Page 01 using the page select digit switches.<br><br>Depress the page display select pushbutton. Observe that there is a W at address 00 on Page 01. See Figure 8.1E | |
| At address 00 on Page 10 an R appears instead of a W. | Check the Record Buffer RAM B13. |
| System will not go into the Page mode. | Check the Front Panel SMD switch for the Page mode. |
| 8.8 Sequential Mode Diagnostic | |
| Select the Sequential display. See Figure 8.1F. Observe that the 11th access is a write (W) access and that the cursor appears under it. | |
| Cursor does not appear under the W access. | Switch back to the Memory mode and verify that the cursor is under the asterisks at Page 01. Check ROM C1. |
| 8.9 List Mode Diagnostic | |
| Select the List display. See | |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
| --- | --- |
| Figure 8.1G. Observe that the cursor appears under the 11th access and that it is a write (W) access. Activate the Select switch. Verify that the accesses appear in binary as shown in Figure 8.1H. | |
| Activating Select switch has no affect on the display. | Check Front Panel SMD switch for the Normal/Select switch. Check ROM C1. |

## 8.10 Page Mode (Program Page 0C) Diagnostic

| | |
| --- | --- |
| Select Page 0C. | |
| Select page display. Verify Figure 8.1I. | |
| Select the Memory Display mode. Move the cursor to Page 0C (under blinking *). The cursor data fields should show the same data as the Stop Event. Verify Figure 8.1J. | |
| Cursor data fields show that data is different to that in the Stop Event. | Check ROM C1. Check that the cursor is under the blinking *. |

## 8.11 Select Operation Diagnostic

| | |
| --- | --- |
| Depress and release the Select switch. Observe that the At Cursor Field shows 17. | |
| Select List mode. Observe that the cursor is located under the second to last access. | |
| Select Memory mode. Depress Select switch and observe that the At Cursor Field is decremented by 1; there is 300 msec pause, and decrementing continues until the At Cursor Field reaches 1, at which time decrementing stops. Observe that the To Cursor Field is equal to 1. | |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| Select Page mode. Observe that the cursor is at the Start Event. Select Sequential mode. Observe that the cursor is at the Start Event. | |
| Select List mode. Observe that the cursor is at the Start Event. | |
| Cursor will not move vertically. Cursor will not decrement to 1, stops short. | Check the Front Panel SMD switch for the vertical movement. Check ROM C1. |

## 8.12 Delayed Stop Event Diagnostic

| | |
|---|---|
| Set the Delay switch to 100. Set the delay modifier to stop. Select the Memory Display mode. Clear the screen. Manually arm the MPA. Reset the SUD. Verify Figure 8.1K. | |
| Select Page display. Verify Figure 8.1L. The Start Event (location 00) and the Stop Event (13) will blink. | |
| Select Sequential display. Observe that the cursor appears at the Start Event. Verify Figure 8.1M. | |
| System not detecting the delay stop command. | Check the Delay switch settings on the Front Panel. Check that the Start/Stop qualifier is in the stop position. Check the RC PCB, the counter that reads the delay switch settings and clocks D2, which supplies the load pulses for the delay counters on the RD PCB. See Figure 9.13, photo 3, for D1 output. See Figure 9.13, photo 4, for D2 output. If the load pulses are not present, the delay settings on the Front Panel will never be loaded into the delay counter. Check D3-6 for DELSTP. |

DIAGNOSTIC PROCEDURE

Use the Select switch in the Sequential position. Depress and release the Select switch. Observe that an S appears at the cursor location and nowhere else. This means that there were no other accesses of location 0C00 during the record sweep.

Move the Select switch to the Normal position. Observe that the S is replaced with the previous symbol (R).

Move the cursor to access 9, depress the Select switch, and verify Figure 8.1N. This shows that there were seven accesses of memory location 0C07 during the record sweep. Put Select switch in the Normal position and release.

Examine RAM write accesses. Move the cursor to access 11. Observe that it is a write access, writing 00 in location 100. Move the cursor down one line. Verify that the second write access writes 01 in location 101. The last write access (107) writes 06 in location 106.

Select Page mode and Page 01. Observe that there are seven write accesses and that the cursor appears at the last write access.

## 8.13 Delayed Start Event Diagnostic

Acquire the following switch positions.

TROUBLESHOOTING PROCEDURE

If these signals are present but delay stop still is not being detected, check the RD PCB for DELO out (D5-6).

If DELO is present, check B10-10 and pin 8.

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| Start Event 0C07<br>Stop Event 0C10<br><br>Delay Modifier Start<br>Delay 8192<br><br>Clear the MPA. Manually arm. Reset the SUD. Switch to the Page mode. Set the Page switch to Page 02. Observe a blinking W at location FF (start event). Observe that there is no * in the start location. See Figure 8.1O. | |
| System does not respond to the Delayed Start Event. Starts at 0C07. | Check that the Delay Start switch is in Start. Verify that the start delay values are loaded into the delay counter on the RD PCB. Check D3-3 on the RC PCB. Check A9-10 and 11 for the correct logic operation. |

## 8.14 Buffer Full LED On/System on a RAM W Access.

Acquire the following switch positions.

| | |
|---|---|
| Start Event | 0C07 |
| Stop Event | 03FF |
| Stop Event Mode | Write |

Manually arm the system. Reset the SUD. The Buffer Full LED will be on. Switch to Page 03. Observe a blinking W at location FF. Move the cursor to location FF and observe the data to be 3F (ASCII). Note that there are 16 write accesses on Page 03. See Figure 8.1P.

| | |
|---|---|
| Buffer Full LED never comes on. | Check RC PCB C9-13. See Figure 9.13, photo 5. If A6-12 goes high and Buffer Full LED stays off, check the Front Panel PCB U14. |

Remove the delay settings and set

the switches as follows:

| | |
|---|---|
| Start Event | 3F3 |
| Stop Event | 3FF |
| Start Event Mode | Write |
| Stop Event Mode | Write |

(Stay in Page mode and observe Page 03.)

Record a Record.

Manually arm the MPA. Verify Figure 8.1Q. The W access at location 3F3 will blink (Start Event) and the X access at location 3FF will also blink (Stop Event).

## 8.15 Auto Arm Diagnostic

Maintain the switch positions as in Figure 8.13. Switch the Arm switch to Auto.

Observe that the MPA arms itself, records a record, and rearms itself at approximately 2 sec intervals.

Observe that the Start and Stop Event data fields are 12 accesses apart and are decremented from 3F to 00. This indicates that the program in the SUD is shifting data through these memory locations.

System fails to auto arm itself and the Start Event LED is off.

Check D4-4 on the RC PCB for the preset pulse. See Figure 9.13, photos 6 and 7. If the pulse is not present, check C9-8 and associated circuitry.

System functions in manual arm but not in auto arm.

Check D4-5 on RC PCB. Check C5-5 if the auto arm FF goes high to low (D4-5).

## 8.16 Delayed Stop/Single Step Diagnostic

Acquire the following switch positions.

| | |
|---|---|
| Start Event Source | Event |
| Start Event Mode | Read |
| Start Event | 0C00 |
| | |
| Delay | 0010 |
| Delay Modifier | Stop |
| | |
| Stop Event Source | Event |
| Stop Event Mode | Read |
| Stop Event | 0C3C |
| | |
| Clear MPA | |
| Record Select | Halt |
| Display Select | Sequential |
| Clear Again | |

Clear and manually arm. The Search for Start Event LED will be on.

Reset the SUD. The MPA will record and stop the 6800 in the SUD. The Record and the Buffer Full LEDs will be on.

Move the cursor to the last access.

Go to List mode. Verify Figure 8.1R. Observe that the last access is 10 accesses away from the Stop Event (0C3C).

Depress and release the Record Control switch. Verify Figure 8.1S. The three accesses following the cursor are the fetch and execution of the LDX immediate instruction in the SUD.

Hold the Record Control switch down and observe the repeat operation. The SUD will go into a five-cycle pause loop that repeats $2^{16}$ times.

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| Record LED goes out after the record sweep. | The system is not entering into the Halt mode or the Record FF is being preset incorrectly. Check B10-9, 8, 6 on RC PCB. A11-6 should be low, keeping the Record LED on via A10-10 to the Front Panel. |
| System fails to execute the single step function. | Check B3-12, 3, and 5 on the RC PCB. As the Single Instruction switch is depressed, B3-3 should output a positive-going pulse. See Figure 9.13, photo 8. |
| System executes one single-step instruction only. | Check B3-13 (reset) on the RC PCB. Check A3-8 |

To check the ability of the system to continue to a new Stop Event and halt the SUD after finding it, set the switches as follows:

Change the Stop Event to 0C21.

Single step at least one more time.

Put the Record Control switch in the Normal position. The MPA will record to the completion of the instruction located at 0C21, which is a RTS.

Go to Sequential and position the cursor at the Stop Event.

Go to list and verify Figure 8.1T.

## 8.17 Manual Start Diagnostic

Set the switches as follows:

| | |
|---|---|
| Start Event Source | External |
| Delay | 0000 |
| Stop Event Source | Event |
| Stop Event Mode | Write |
| Stop Event | 0100 |
| Record Select | Normal |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| Clear the MPA. Manually arm it. Push up and release the Manual Start/ Stop switch. Observe that the buffer Full LED is on.<br><br>Go to Sequential. Move the cursor to the Stop Event. Observe that it is a Write in location 0100.<br><br>New Switch settings:<br><br>Start Event Source Event<br>Start Event Mode Read<br>Start Event 1C00<br><br>Clear the MPA. Manually arm it. Push up and release the Manual Start/Stop switch. Observe that the Buffer Full LED is on.<br><br>Go to Sequential. Move the cursor to the Stop Event. Observe that it is a Write in Location 0100. | |
| Pressing Manual Start fails to start a record process. | Check D6-8 on the RC for a high-going level. If pin 8 goes high, check pin 10. If these levels are correct, check B5-4. See Figure 9.13, photo 9. Manual Start comes from the Front Panel. C2 or RC PCB forms the switch output into a pulse that presets A11-5 high. Check B12-3. |

## 8.18 Manual Stop Diagnostic

Set the switches as follows:

Start Event Source Event
Start Event Mode Read/Write
Start Event 0C25

Stop Event Source Event
Stop Event Mode Write
Stop Event 1100
Display Mode List

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| Manually arm the MPA. Observe that the Stop Event Search, Record, and Buffer Full LEDs are on. | |
| Depress and release the Manual Start/Stop switch. Observe that the data on the CRT is valid. | |
| Manual Stop fails to stop recording. | Check input to D6-12 on the RC PCB. Pin 13 should be a high-going level when the Stop switch is depressed. If pin 13 is correct, check A10-2 for a low-going pulse that should preset A11-9 high. With A11-5 low, recording terminates and the Stop Event and Record LEDs go out. |

## 8.19 EOS Diagnostic

To qualify the EOS command, the Stop Event switch setting must be greater than 256 accesses deep into the program (SUD). Otherwise, the MPA will record to the selected Stop Event and not record to the end of storage if that setting is less than 256 accesses.

Set the switches as follows:

| | |
|---|---|
| Stop Event | 1C00 |
| Stop Event Source | EOS |

Clear the MPA
Manually Arm

Observe that the Buffer Full LED is on and the Start Event is a read access of location 0C25.

| | |
|---|---|
| System never recognizes an EOS event because Buffer Full LED never comes on and system outputs erroneous data. | Check A9-2, 13 on the RC PCB. Pins 2 and 13 should be high. Pin 1 should be low and go high as a result of ADRTC and SUDCP1 being |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| | high together. See Figure 9.13, photo 10.<br><br>Check the address counters on the RD PCB if ADRTC is not present. |

## 8.20 Loop Iteration Diagnostic

Set the switches as follows:

| | |
|---|---|
| Display Mode | List |
| Start Event | 0C03 |
| Source | Event |
| Mode | R/W |
| | |
| Stop Event | 0C11 |
| Source | Event |
| Mode | R/W |
| | |
| Delay | 0000 |
| Record | Normal |

Connect a frequency counter to the Stop Event Output BNC. Set the counter to the Totalize mode. Clear the MPA. Switch the Record switch to Halt. Clear again. Switch the Arm switch to the Auto mode. Reset the counter. Reset the SUD. The counter should count to 768 and stop.

CRT indicates that the system is going through the loop but there are no Stop Event pulses from the output BNC.

Check A10-6 on the RC PCB low-going pulses. If A10-6 is present, check U21-3 and 4 on the Front Panel board.

## 8.21 Start, Stop, and Delayed Start/Stop Event Output Diagnostic

Set the switches as follows:

| | |
|---|---|
| Delay | 0000 |
| Delay Modifier | Start |
| Start Event | 0C25 |
| Stop Event | 0C26 |
| Stop Event Mode | Read |
| Stop Event Source | Event |

Put the Arm switch in the Auto position. Connect an 851-D logic recorder to the Start, Stop, and Delayed Start/Stop Event output BNCs. Trigger on Channel 1 going positive. Use Pretrigger Record mode, delay of 10, internal clock; 0.02 µsec, X5, mixed, with cursor all the way to left. Verify Figure 8.1U. The Start Event and Start Event Delayed pulses occur almost simultaneously and the Stop Event pulse occurs approximately 2.0 µsec later.

Change switch settings as follows:

| | |
|---|---|
| Delay Modifier | Stop |

Verify Figure 8.1V. Controls on 851-D do not change.

Change switch settings as follows:

| | |
|---|---|
| Delay | 0001 |
| Delay Modifier | Start |

Verify Figure 8.1W.

This tests the delaying of the Stop Event by one clock cycle. Change switch settings as follows:

| | |
|---|---|
| Delay | Stop |

851-D internal clock to 0.05 µsec.

Verify Figure 8.1X.

This tests the delaying of the Start Event by 10 cycles. Change switch settings as follows:

| | |
|---|---|
| Delay Modifier | Start |
| Delay | 10 |
| Stop Event | 0C33 |

851-D internal clock to 0.2 µsec.
851-D multiplexer to X1.

Verify Figure 8.1Y.

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| This tests the delaying of the Stop Event by 10 cycles. Change switch settings as follows: | |
| Delay Modifier Stop | |
| 851-D internal clock to 0.2 µsec. | |
| Verify Figure 8.1Z. | |
| External output pulses missing. | Check the RC PCB gates A6-8 STAOT, A10-10 STPOT, and A6-10 DISSOUT. See Figure 9.13, photo 11, for the Delayed Start Logic path. See Figure 9.13, photo 12, for the Delayed Stop path. |

## 8.22 Supplementary Peripheral Diagnostic Procedure

The following diagnostic procedures are added as supplements to the preceding procedures. These procedures need not be performed as a part of the maintenance procedure on the 168-D.

The various failure modes introduced are hypothetical. These modes are intended to provide additional information for the analysis, understanding, repair, and maintenance of the 168-D.

Failure modes presented in this section do not represent a deficiency in system reliability. However, care should be used when analyzing the circuitry.

## 8.23 MPU PCB and Hypothetical Failures

The MPU PCB contains the APAGE RAM and the ROM along with the Microprocessor itself. Therefore, system management originates via the MPU PCB. Also, the clock network that supplies the CCRT clock, Phase 1 and Phase 2 clock, CPP1 and CPP2 originates from this PCB.

| DIAGNOSTIC PROCEDURES | TROUBLESHOOTING PROCEDURES |
| --- | --- |
| When power (AC) is turned on, the screen remains black. No display is present. | Check the clock input to J6-2. See Figure 9.9, photo 1. See Figure 9.9, photo 2, for CCRT. |
| Screen displaying snow. | See Figure 8.2A. Review Figure 9.9, photos 1 and 2. The CCRT clock should be 4.4016 MHz. If CCRT is off, the timing for the complete system will be off and the display will be similar to that of Figure 8.2A.<br><br>Check the crystal frequency (22.008 MHz). Check clock network K8. Check the counters J6 and J8. Check K7. See Figure 9.9, photo 3, for CCP1, 2, phases 1 and 2. |
| From a power-up state, erroneous data is printed on the screen. | See Figure 8.2C as an example of incorrect character display from a power-up state. This represents a type of display that could result if an address line is low as a result of an output bus driver going bad. In this example, E6-8 was held low. As a result, the restart vector was never found. |
| From a power-up state, erroneous data is printed along with incorrect display modes. | See Figure 8.2B. In this example, H6-3 was held low during a power-up start. A13 (address line), as a result, was low. The system came up in the Memory mode but was programmed to be in the List mode. Data should not be displayed in the quadrants. The correct system start as a function of the software issues a clear screen command. |

DIAGNOSTIC PROCEDURE

TROUBLESHOOTING PROCEDURE

## 8.24 MPU RAM Diagnostic

Turn off the AC power to the system. Remove the MPU PCB. Replace the C1 ROM with the Shift Program ROM. Lift up the Record Control and Data PCBs from their sockets. Insert the MPU PCB back into its socket. Turn on the AC power. Observe Figure 8.2D. This program shifts all the ASCII characters through the RAM storage area 0100-3FF (256-1023). The CRT driver reads from these locations and displays the data therein.

CRT display (recorded data, fixed field data) does not correspond to appropriate data that should be displayed.

Observe Figure 8.2D. Inspect location 0100, upper left-hand corner of the picture. The ASCII upper case K is stored there. Scan the column vertically. Observe that every other character is a K. Observe the lower right-hand corner of the picture location 3FF. The character J is present. This character is shifted into the first CRT location on the screen (0100). Therefore, at the same time there is a J in location 3FF, there should be a K in location 0100. If at the same time there was a J at location 3FF and 0100, then the output from RAM A5 at this particular time would be incorrect.

Offering another possible means of analyzing the RAM memory is the RAM program. Turn off the AC power to the system and insert the RAM program into location C1. Observe Figure 8.2E as it depicts the program as it alternately writes and reads a checkerboard

pattern and its complement into RAM locations 0 through 3DF (not the last line of the display) and pauses for approximately 2 sec. The address and the data read from that address are displayed on the last line of the display. If the data read does not agree with that which was written and an * is displayed, the error address in RAM memory is displayed, and the bit pattern at that location is displayed in hexadecimal. If the RAM are good the comparison error at the bottom of the display should not stop. See Figure 8.2F depicting a simulated bad RAM.

## 8.25 CRT Driver Diagnostic

Review the following for problems relating to display of data.

| | |
|---|---|
| Blank screen. | Check Q1-E. See Figure 9.7, photo 1. This is the composite video output to the CRT PCB. If the top half of the envelope in Figure 9.7, photo 1, is missing, the screen is void of data.<br><br>If the horizontal or vertical synchronization signal are low, the screen is blank. If the output from C1 (the Video Shift Register) is low, the screen is blank.<br><br>If LBCP (line buffer clock pulse) is low, the screen is blank. |
| Cursor missing. | See Figure 8.2G depicting the cursor missing under Page 0C. Check D4-12. Check the output of D3-12 and the output of B2-5. |
| Characters not blinking. | Check the output of D4-11 and the associated circuitry. |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| Blank screen with cursor only. | See Figure 8.2H. Check the clock to the Row Counter D2-2. See Figure 9.7, photo 2, for the CPRCT clock. |
| Improper print out of data on the CRT screen. | See Figure 8.2I. Check the Line Buffer E4, the Character Generator E1, the Video Shift Register C1, and the Row Counter D2. |

## 8.26 Record Data PCB Diagnostic

Review the following for problems relating to the Record Data PCB.

| | |
|---|---|
| System experiencing problems relating to loading the control words for switch positions on the Front Panel. | Check D10 and associated circuits. |
| Start and/or stop addresses incorrect on CRT display. | Check D15, 14, 13 and 12 for the Start Event. Check C16, 15, 14, and 13 for the Stop Event.<br><br>Check B17, 16, 15, and 14.<br><br>Check the address counters C5 and C8. |
| System incorrectly processing the delay setting. | Check the delay counters D1, 2, 3, and 4. |
| System not detecting the SUDESI signal. | Check D11. |
| System recording data incorrectly. | Check C1 and associated circuits. |

## 8.27 Record Control PCB Diagnostic

Review the following for problems relating to the RC PCB.

| | |
|---|---|
| Manual Start fails. | Check B7 and associated circuits. |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
| --- | --- |
| System fails to clear CRT when the Clear switch is on. | Check to see if the halt qualifier is switched on. If so, the system will not clear.<br><br>If the system is in the Normal mode and still will not clear, check A8-11. |
| System recording erroneous data. | See Figure 8.2J and compare it to 8.2K. Check the 6800 clock circuit C11-12. See Figure 9.13, photo 13. |
| Replace the 6800 SUD with the 8080 SUD to verify that the circuits for the 8080 SUD function.<br><br>Acquire the following system positions:<br><br>Start Event Source — Event<br>Start Event Mode — R/W<br>Start Event — 0000<br><br>Stop Event Source — Event<br>Stop Event Mode — R/W<br>Stop Event — 0008<br><br>Record Select — Normal<br>Record Control — Normal<br>Display Select — List<br>Access — µP<br>Arm — Auto<br><br>PM switches S1-S8 on; S9 and S10 off.<br><br>Turn on MPA and 8080 SUD power.<br><br>Clear MPA and 8080 SUD.<br><br>Verify Figure 8.3A and Start Event will blink.<br><br>Turn PM switch S9 to ON; verify Figure 8.3B and observe data and addresses. | |
| System fails to record. | Check C10-8 for the clock pulses for the 8080. Check |

| DIAGNOSTIC PROCEDURE | TROUBLESHOOTING PROCEDURE |
|---|---|
| | D12-8. Check that $\overline{\text{SUDIC}}$ is high (B4-4). |
| System fails to record the status at SYNC time. | Check D10-5 and 6. With the switch on the 8080 personality module on, a high should enable the SYNC signal to pin 4. |

## 8.28 Disassembly Procedure

The following are the disassembly procedures for the top cover, bottom cover, front panel, power supply, and CRT assembly. Tools needed to perform these disassemblies are a phillips head screw driver and a nut driver set with at least a 6-inch extension.

### 8.28.1 Top Cover Disassembly

Removing the top cover requires extracting two screws at the top-back portion of the 168-D. After removing the two screws, slide the cover back and lift up.

### 8.28.2 Bottom Cover Disassembly

Remove the AC power line to the 168-D. Tilt the system on end (side with the fan and AC connection). Remove all six screws on the bottom of the system.

### 8.28.3 Front Panel Disassembly

To disassemble the Front Panel, the top cover must first be removed. Refer to Figure 9.29 for the hardware location. Remove the items depicted in Figure 9.29.

If the AC line is connected as might be the case for troubleshooting the Front Panel, use care when laying the Front Panel assembly on its face. The AC switch might switch on unexpectedly.

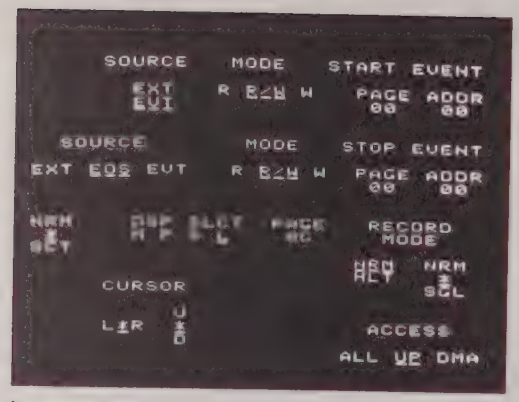
### 8.28.4 Power Supply Disassembly

Remove the top cover. Refer to Figure 9.29 as it depicts the location of two of the seven items to be removed. Observe the system from the top. Six of the seven items are on the bottom of the power supply and the brace is at the top. Remove the hardware and disconnect the cable connections to the assembly.

### 8.28.5 CRT Section Disassembly

Remove the top cover. Refer to Figure 9.29 as it depicts the location of two of the four items to be removed. Observe the CRT

section from the top and remove the four items. Make sure the AC power is off before attempting this disassembly procedure. Disconnect the cable to the PCB. Lift the assembly out of the chassis using care. DO NOT DROP OR BUMP THE CRT TUBE - IT MAY IMPLODE AND CAUSE BODILY INJURY.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MODE
START EVENT
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EVT
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SOURCE
MODE
STOP EVENT
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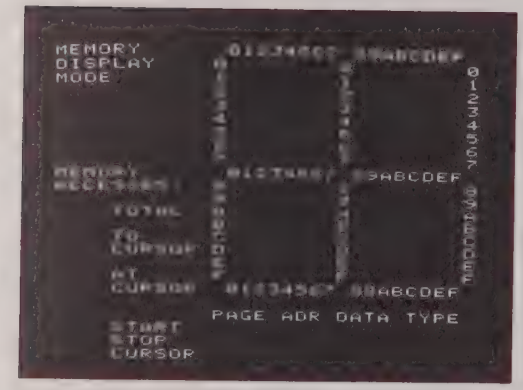
A.


MEMORY
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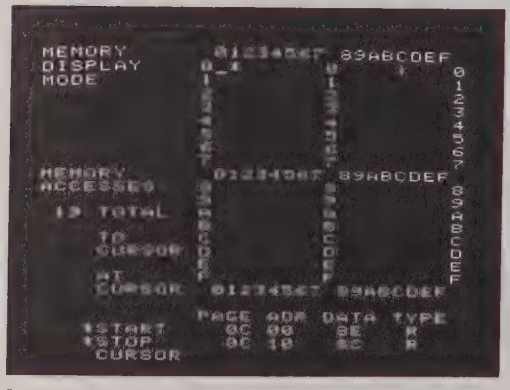
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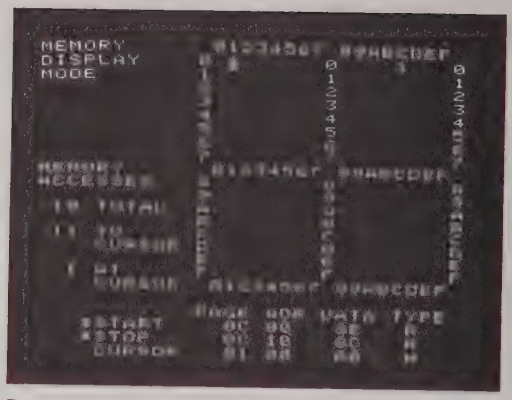
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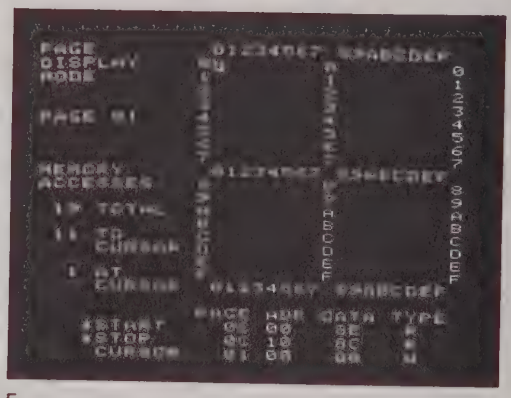
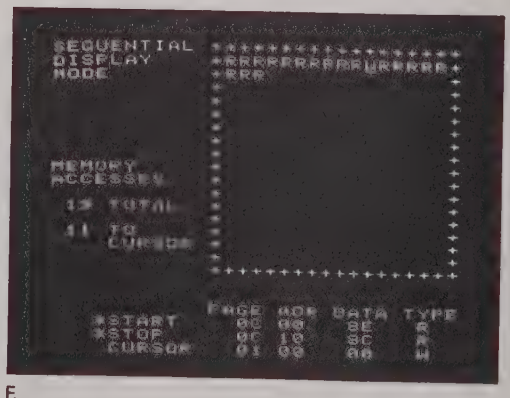
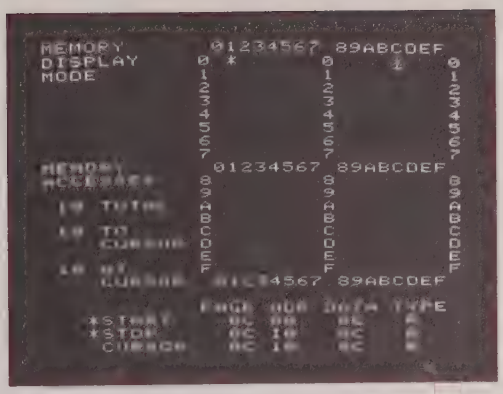

PAGE
DISPLAY
MODE
PAGE 01
MEMORY
ACCESSES
TOTAL
TO
CURSOR
AT
CURSOR
PAGE ADR DATA TYPE
*START
*STOP
CURSOR

E.


SEQUENTIAL
DISPLAY
MODE
MEMORY
ACCESSES
TOTAL
TO
CURSOR
PAGE ADR DATA TYPE
*START
*STOP
CURSOR

F.

G.



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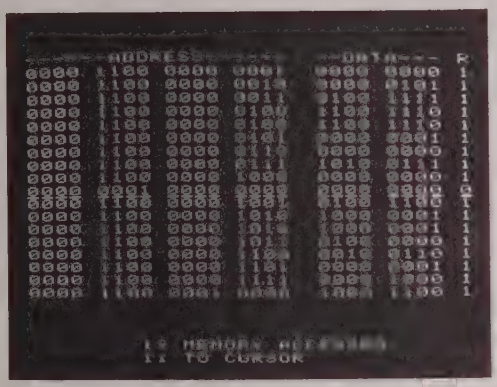

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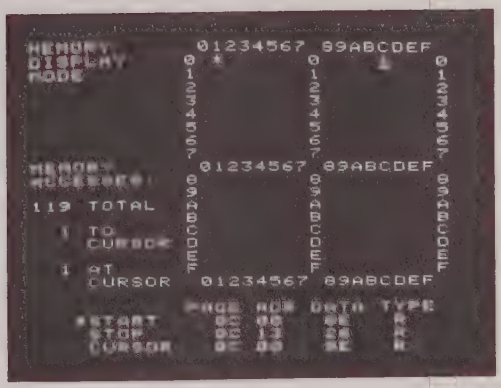
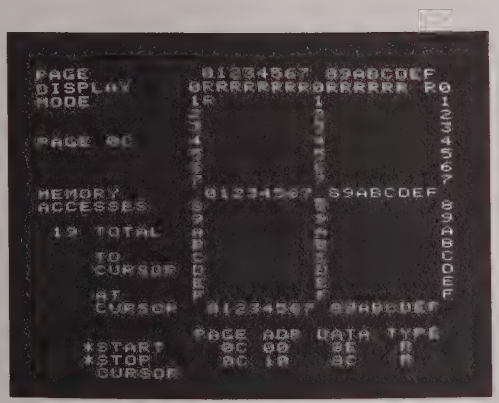


K.



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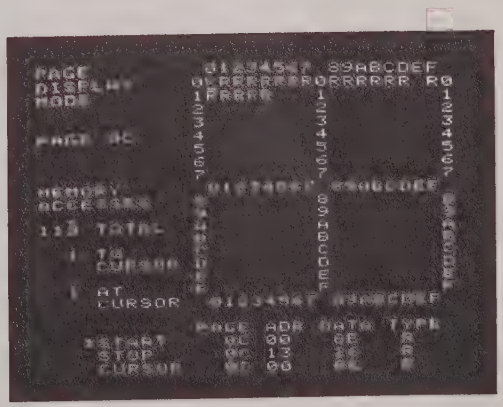
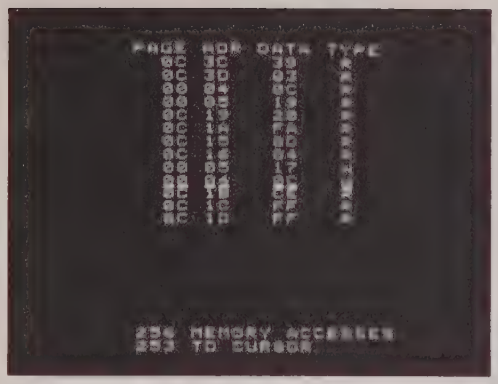
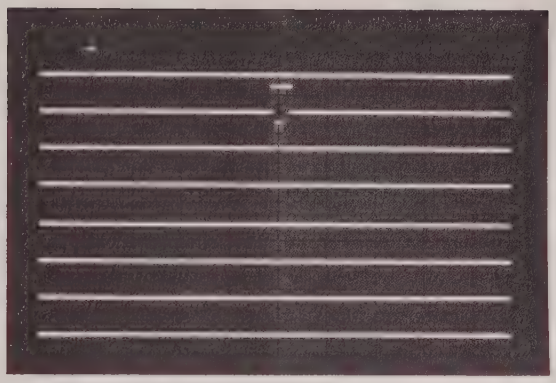


L.

Figure 8.1 Waveform Photographs
A-L




S.



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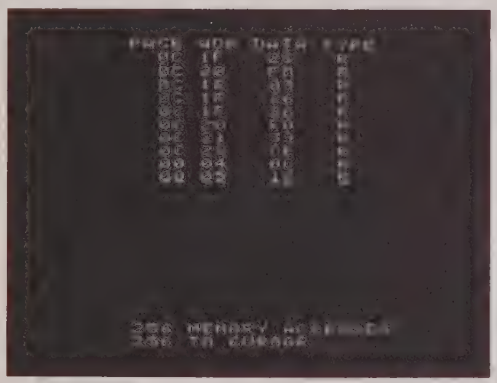
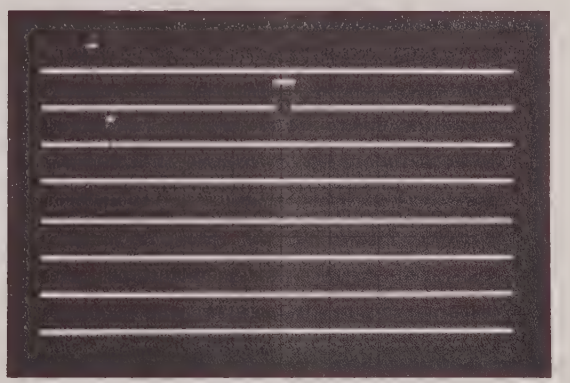
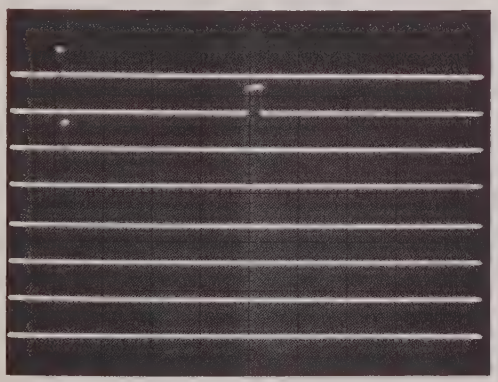


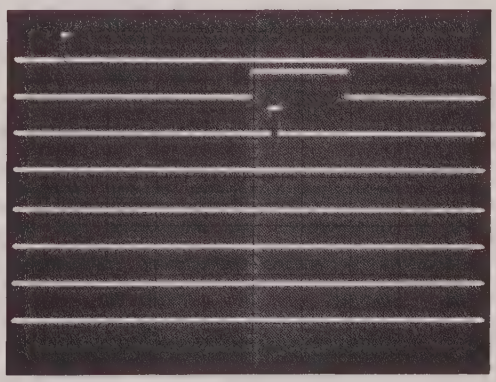
T.



W.

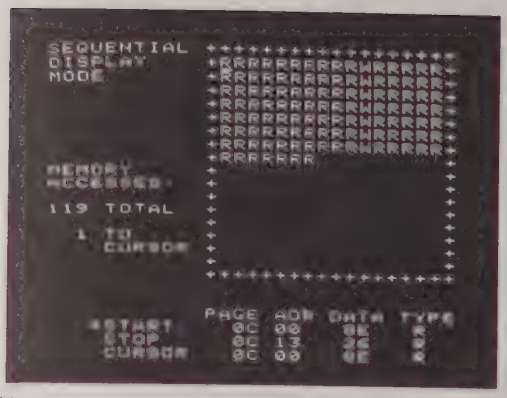


U.

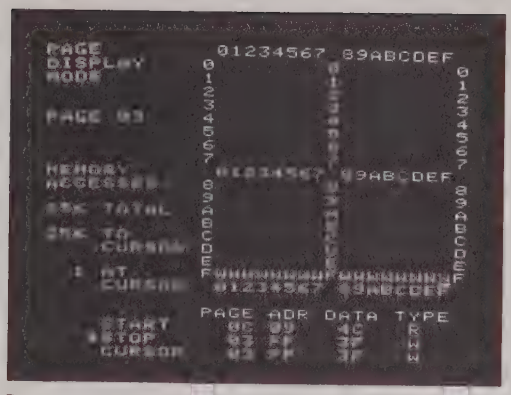


X.

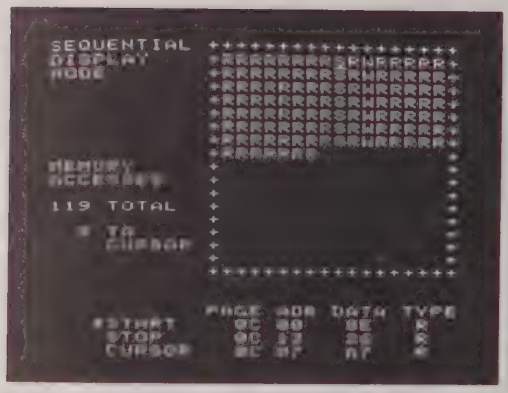
Figure 8.1 Waveform Photographs
M-X


SEQUENTIAL
DISPLAY
MODE
MEMORY
ACCESSES:
119 TOTAL
1 TO
CURSOR
PAGE ADR DATA TYPE
*START 0C 00 0E R
STOP 0C 13 26 R
CURSOR 0C 00 0E R

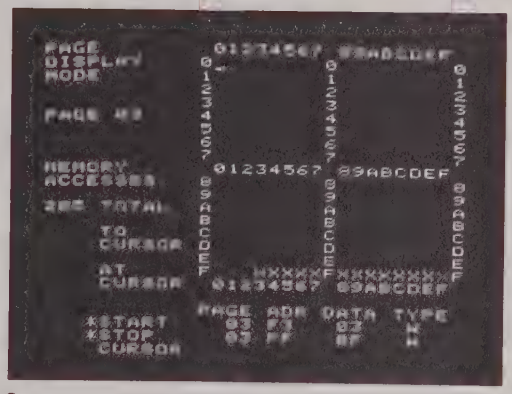
M.


PAGE
DISPLAY
MODE
PAGE 03
MEMORY
ACCESSES
256 TOTAL
256 TO
CURSOR
1 AT
CURSOR
PAGE ADR DATA TYPE
*START 0C 00 4C R
STOP 03 FF 3F W
CURSOR 03 FF 3F W

P.


SEQUENTIAL
DISPLAY
MODE
MEMORY
ACCESSES
119 TOTAL
1 TO
CURSOR
PAGE ADR DATA TYPE
*START 0C 00 0E R
STOP 0C 13 26 R
CURSOR 0C 0F 0F R

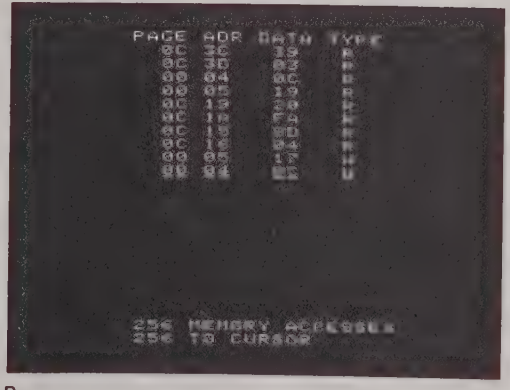
N.


PAGE
DISPLAY
MODE
PAGE 03
MEMORY
ACCESSES
256 TOTAL
TO
CURSOR
AT
CURSOR
PAGE ADR DATA TYPE
*START 03 F3 02 W
*STOP 03 FF 0F W
CURSOR

Q.

PAGE
DISPLAY
MODE
PAGE 02
MEMORY
ACCESSES
31 TOTAL
1 TO
CURSOR
1 AT
CURSOR
PAGE ADR DATA TYPE
START 02 FF 3F W
*STOP 0C 10 00 R
CURSOR 02 FF 3F W

O.


PAGE ADR DATA TYPE
256 MEMORY ACCESSES
256 TO CURSOR

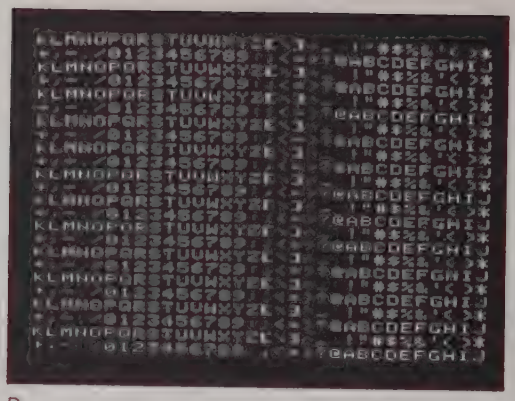
R.

Y.

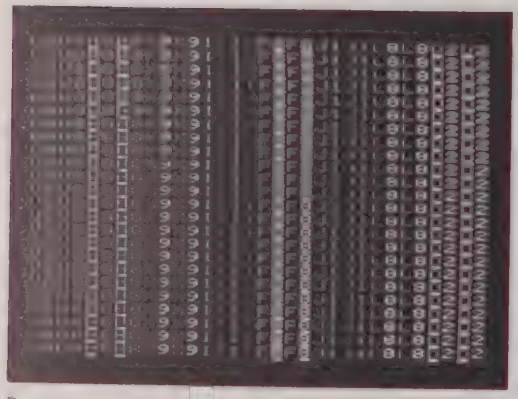
Z.

Figure 8.1 Waveform Photographs
Y-Z

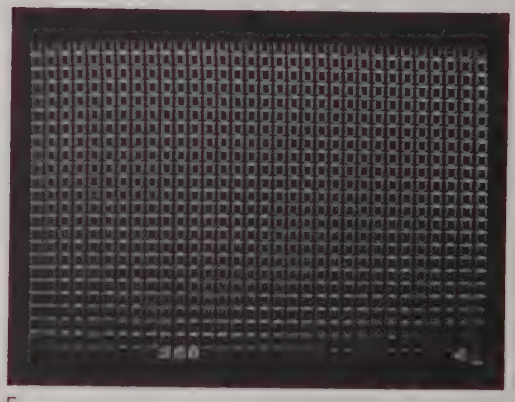
A



D.



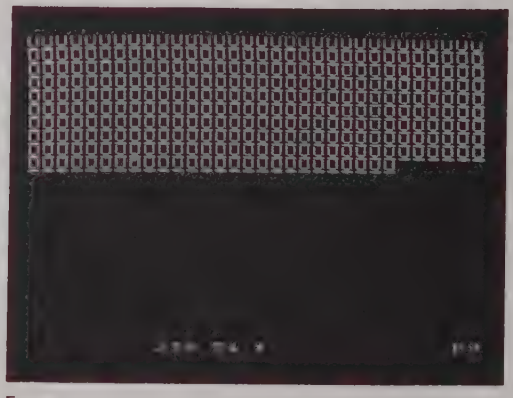
B



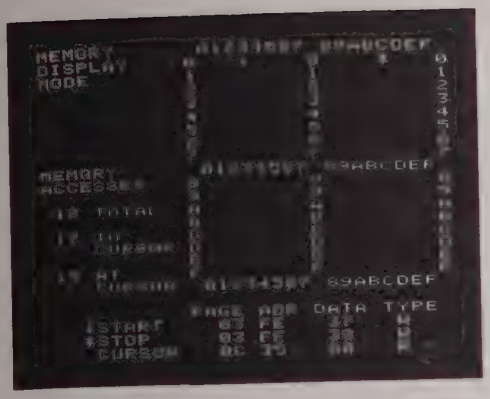
E.

MEMORY
DISPLAY
MODE
MEMORY
ACCESSED
838 TOTAL
154 TO
CURSOR
PHASE ADR DATA TYPE
START
STOP
CURSOR

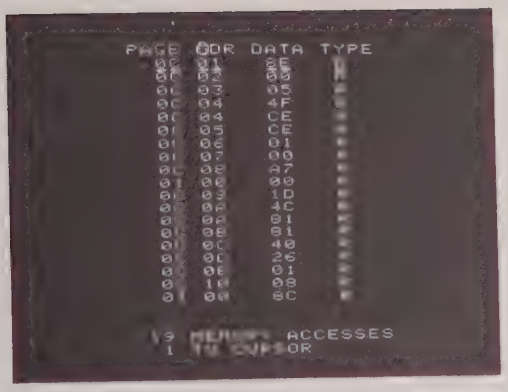
C.



F.

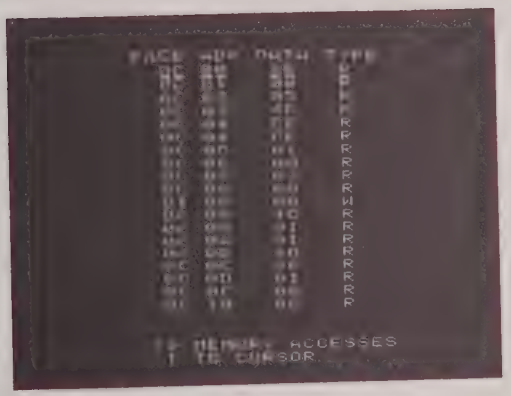


G.

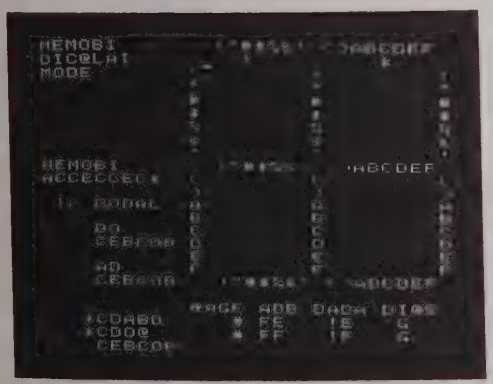



J.

H.



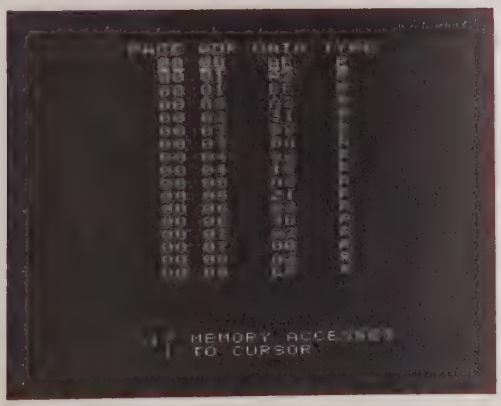
K.



I.

Figure 8.2 Waveform Photographs
A-K

A.




B.

Figure 8.3 Waveform Photographs
A-B

# SECTION IX

# SCHEMATICS AND ASSEMBLY DRAWINGS

## 9.1 Introduction

This section contains the schematics and assembly drawings for the Model 168-D. In addition, there are pictorial diagrams of the assemblies showing locations of adjustment and test points.

## 9.2 List of Drawings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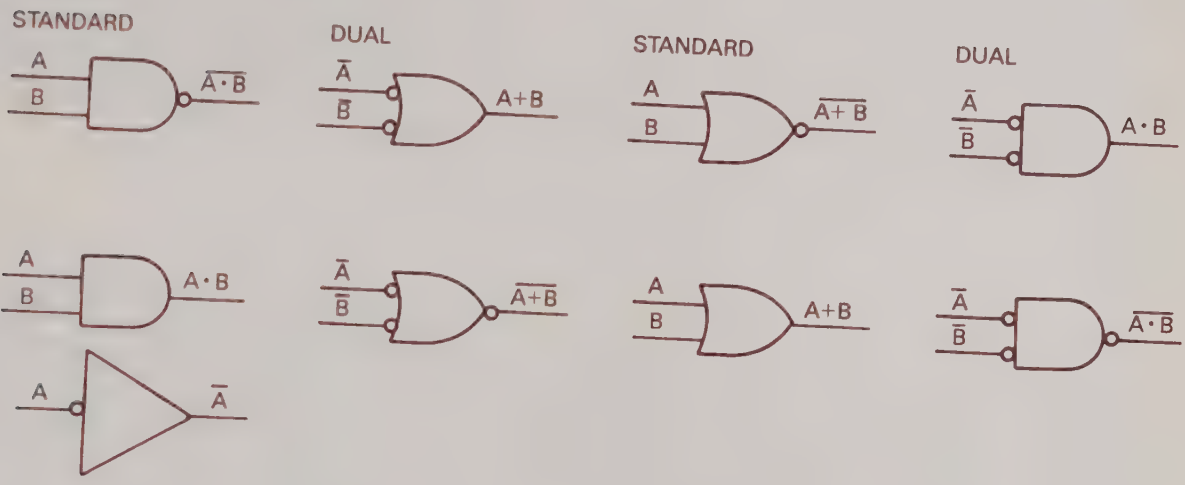
## Logic Symbols

The Logic Symbols used in this manual depict the logic function performed and may be different than those published in the manufacturers' data books.

For example:




## Reference Designators

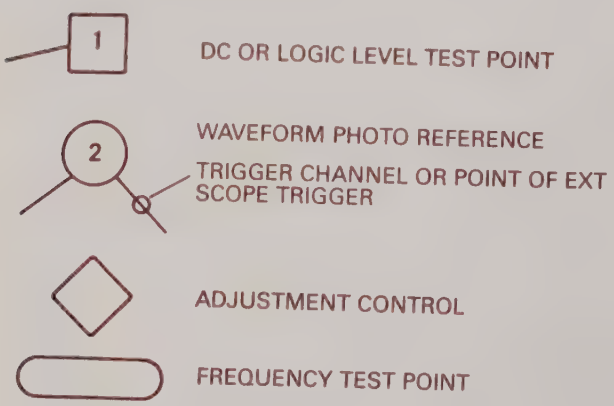



Figure 9.1 Logic Symbols and Reference Designators

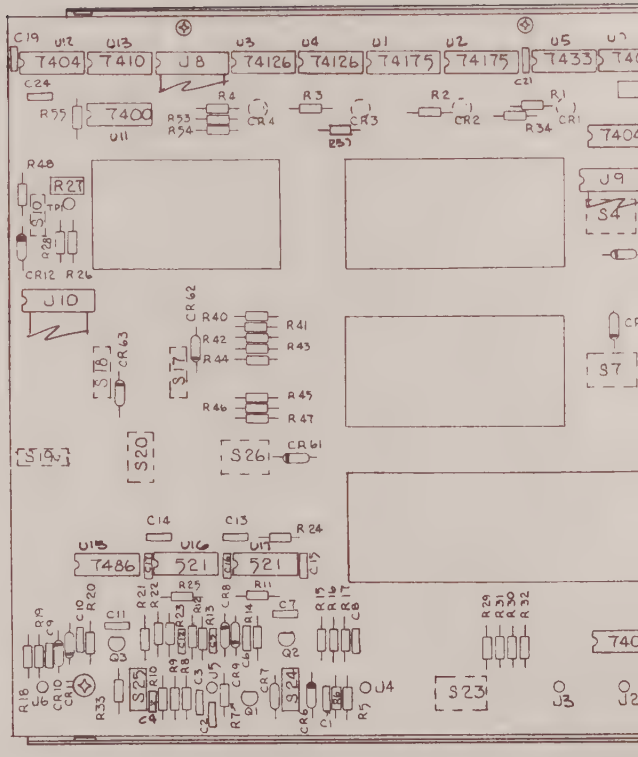

U12
U13
U3
U4
U1
U2
U5
7404
7410
J8
74126
74126
74175
74175
7433
C19
C24
C21
R55
7400
U11
R4
R3
R2
R1
R33
R34
CR4
CR3
CR2
CR1
R48
R27
S10
R28
CR12
R26
J10
CR62
R40
R41
R42
R43
R44
CR63
S18
S17
R45
R46
R47
S20
S26
CR61
C14
C13
R24
U18
U16
U17
7486
521
521
C15
R25
R11
R21
R22
R23
R12
R13
R14
R15
R16
R17
C8
R29
R31
R30
R32
R9
C9
C10
R20
R10
R8
C3
C4
C5
C6
C7
C8
R33
R7
R5
S25
S24
S23
J4
J5
J3
J2
R18
CR10
CR11
CR5
CR6
CR7
J9
S4
S7

Figure 9.2 PCB Front Panel Assembly Drawing

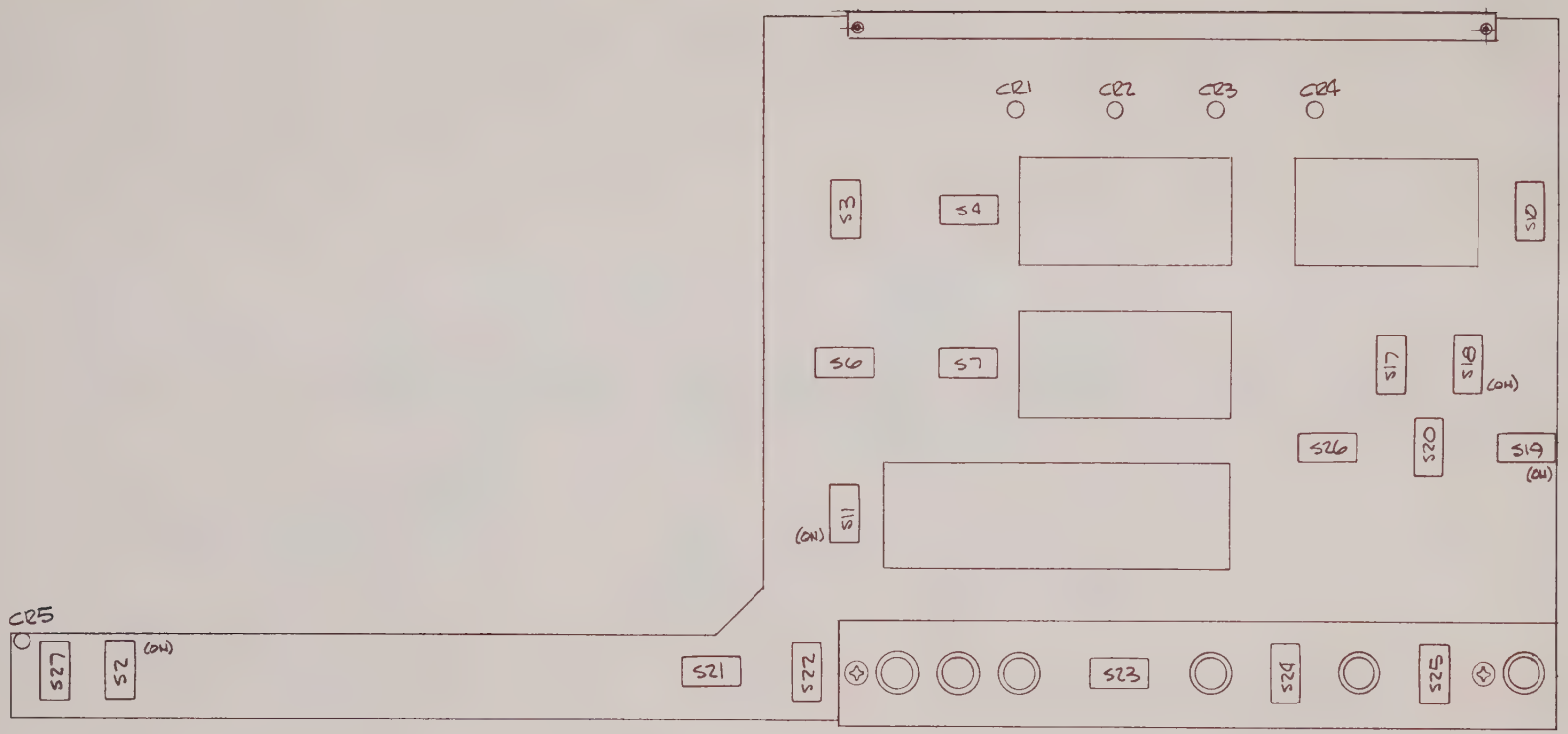



Figure 9.3 PCB Front Panel Assembly Drawing

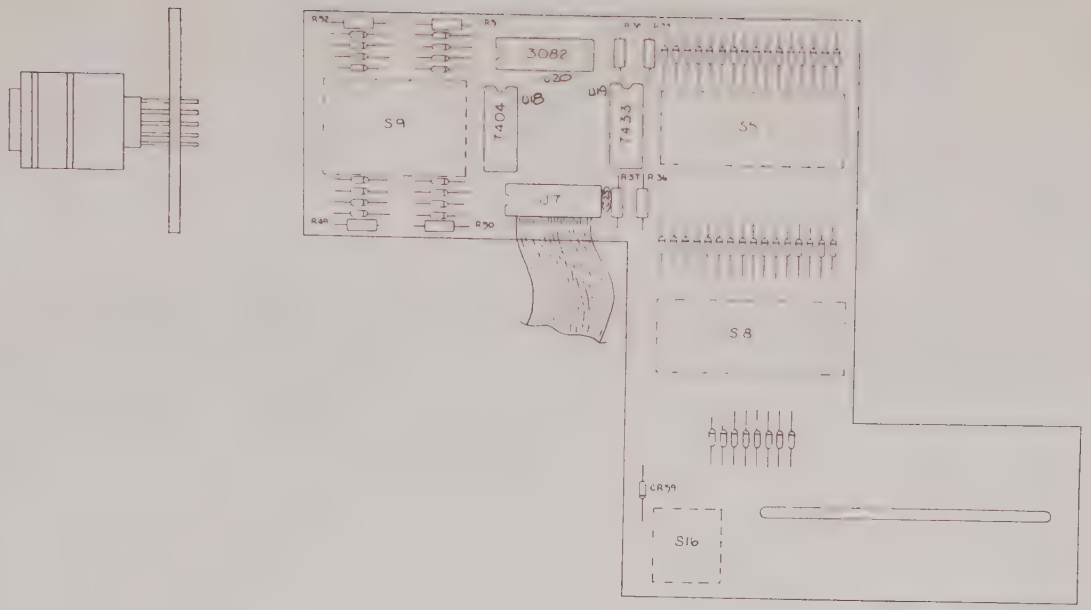
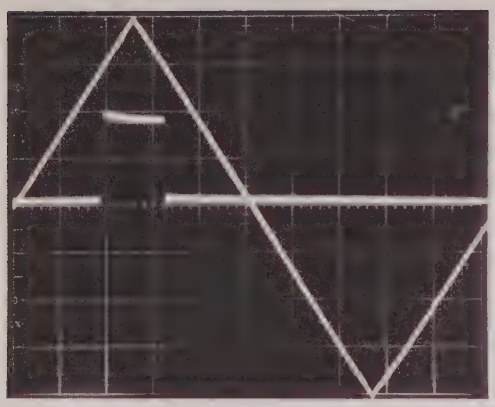
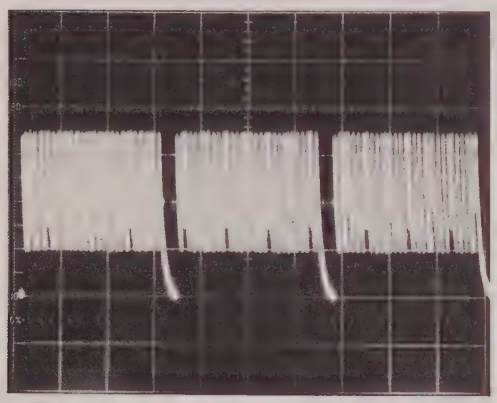



Figure 9.4 PCB Thumbwheel Assembly Drawing



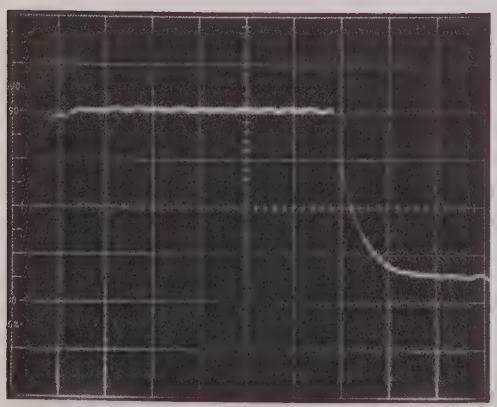
1. Vert. 1 V/cm
Horiz. 2 μsec/cm
CH.A 8 V pp, 50 kHz Triangle Waveform
CH.B C5-13 Record Control Board

TO MPU



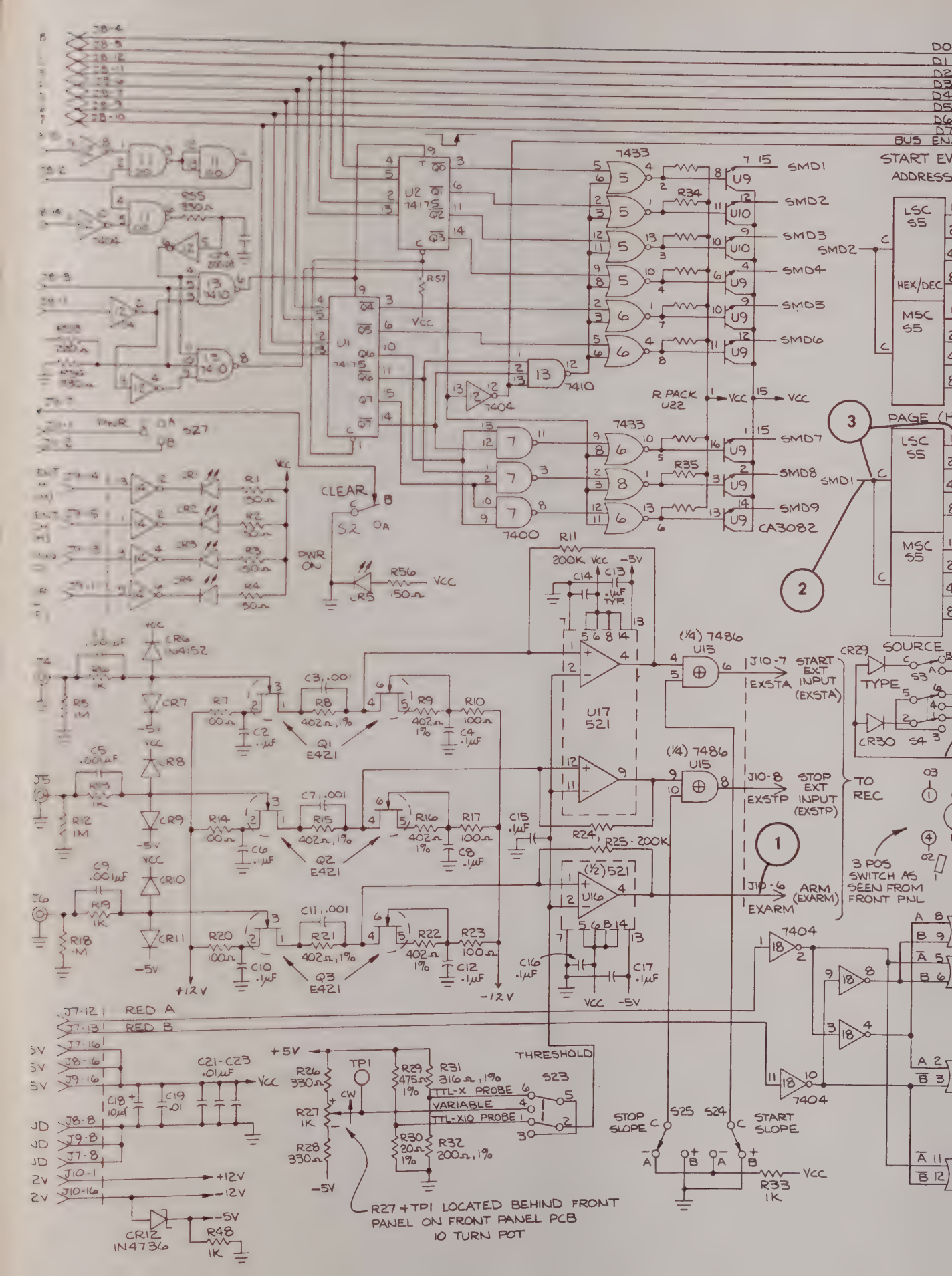
2. Vert. 1 V
Horiz. 5 msec/cm
Int. Trig. (+) Norm

TO REC



3. Vert. 1 V
Horiz. 0.1 μsec/cm
Int. Trig. (+)

TO REC


D0
D1
D2
D3
D4
D5
D6
D7
BUS EN
START EV
ADDRESS
U2 74175
U1 74175
7433
7410
7404
7400
SMD1
SMD2
SMD3
SMD4
SMD5
SMD6
SMD7
SMD8
SMD9
R PACK U22
CA3082
LSC S5
HEX/DEC
MSC S5
PAGE (H
CLEAR
S2
PWR ON
CR5
R56 150Ω
VCC
R11 200K
C14 C13 .1μF TYP.
U17 521
(1/4) 7486 U15
J10-7 START EXT INPUT (EXSTA)
EXSTA
J10-8 STOP EXT INPUT (EXSTP)
EXSTP
J10-6 ARM (EXARM)
EXARM
TO REC
SOURCE
TYPE
CR29
CR30
S3
S4
3 POS SWITCH AS SEEN FROM FRONT PNL
R24
R25 200K
(1/2) 521 U16
C15 .1μF
C16 .1μF
C17 .1μF
C3 .001
C7 .001
C11 .001
Q1 E421
Q2 E421
Q3 E421
R8 402Ω 1%
R15 402Ω 1%
R21 402Ω 1%
R9 402Ω 1%
R16 402Ω 1%
R22 402Ω 1%
R10 100Ω
R17 100Ω
R23 100Ω
C4 .1μF
C8 .1μF
C12 .1μF
CR6 IN4152
CR7
CR8
CR9
CR10
CR11
+12V
-12V
-5V
VCC
RED A
RED B
THRESHOLD
TP1
R26 330Ω
R27 1K
R28 330Ω
R29 475Ω 1%
R31 316Ω 1%
R30 20Ω 1%
R32 200Ω 1%
TTL-X PROBE
VARIABLE
TTL-X10 PROBE
S23
S24
S25
STOP SLOPE
START SLOPE
R33 1K
C18 10μF
C19 .01
C21-C23 .01μF
CR12 IN4736
R48 1K
7404
R34
R35
R11
R1
R2
R3
R4
R5
R12
R18
R9
R14
R20
R6
R7
R13
R19
R8
R15
R21
R16
R22
R10
R17
R23
C1
C2
C5
C6
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C21-C23
J5
J6
J7
J8
J9
J10
S27
RS5
RS7
RS8
RS9
RS10
RS11
RS12
RS13
RS14
RS15
RS16
RS17
RS18
RS19
RS20
RS21
RS22
RS23
RS24
RS25
RS26
RS27
RS28
RS29
RS30
RS31
RS32
RS33
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R PACK U22
CA3082
R1 50Ω
R2 50Ω
R3 50Ω
R4 50Ω
R5 1M
R6 1K
R7 100Ω
R8 402Ω 1%
R9 402Ω 1%
R10 100Ω
R11 200K
R12 1M
R13 1K
R14 100Ω
R15 402Ω 1%
R16 402Ω 1%
R17 100Ω
R18 1M
R19 1K
R20 100Ω
R21 402Ω 1%
R22 402Ω 1%
R23 100Ω
R24
R25 200K
R26 330Ω
R27 1K
R28 330Ω
R29 475Ω 1%
R30 20Ω 1%
R31 316Ω 1%
R32 200Ω 1%
R33 1K
R34
R35
R48 1K
C1 .001μF
C2 .1μF
C3 .001
C4 .1μF
C5 .001μF
C6 .1μF
C7 .001
C8 .1μF
C9 .001μF
C10 .1μF
C11 .001
C12 .1μF
C13 .1μF TYP.
C14 .1μF TYP.
C15 .1μF
C16 .1μF
C17 .1μF
C18 10μF
C19 .01
C21-C23 .01μF
CR5
CR6 IN4152
CR7
CR8
CR9
CR10
CR11
CR12 IN4736
CR29
CR30
S2
S3
S4
S23
S24
S25
U2 74175
U1 74175
U9
U10
U15
U16
U17 521
7433
7410
7404
7400
LSC S5
HEX/DEC
MSC S5
SMD1
SMD2
SMD3
SMD4
SMD5
SMD6
SMD7
SMD8
SMD9
CLEAR
PWR ON
VCC
+12V
-12V
-5V
+5V
RED A
RED B
THRESHOLD
TP1
TTL-X PROBE
VARIABLE
TTL-X10 PROBE
STOP SLOPE
START SLOPE
START EXT INPUT (EXSTA)
STOP EXT INPUT (EXSTP)
ARM (EXARM)
TO REC
SOURCE
TYPE
3 POS SWITCH AS SEEN FROM FRONT PNL
R27 + TP1 LOCATED BEHIND FRONT PANEL ON FRONT PANEL PCB 10 TURN POT
Q1 E421
Q2 E421
Q3 E421
1
2
3
J10-7
J10-8
J10-6
EXSTA
EXSTP
EXARM

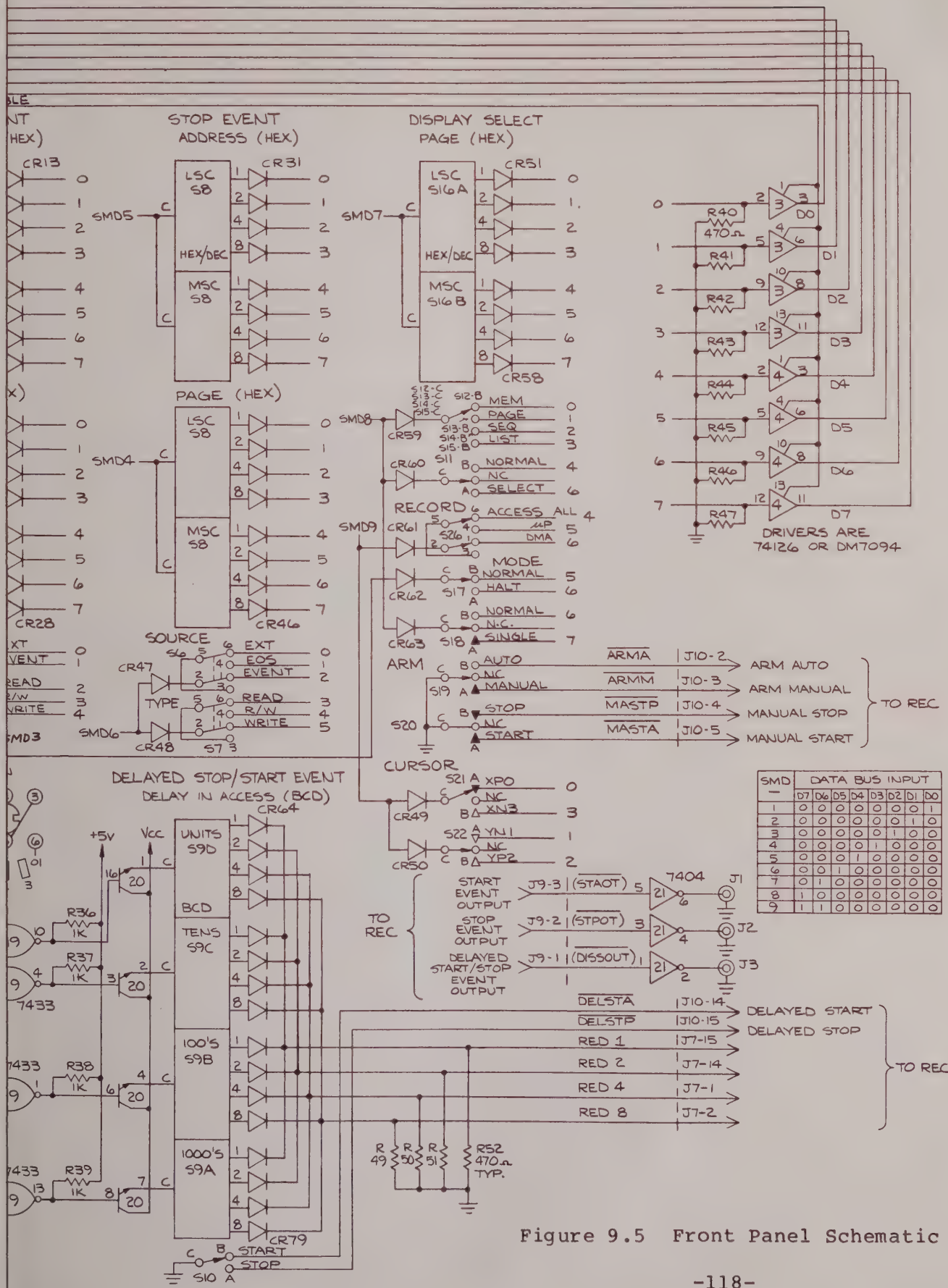



Figure 9.5 Front Panel Schematic

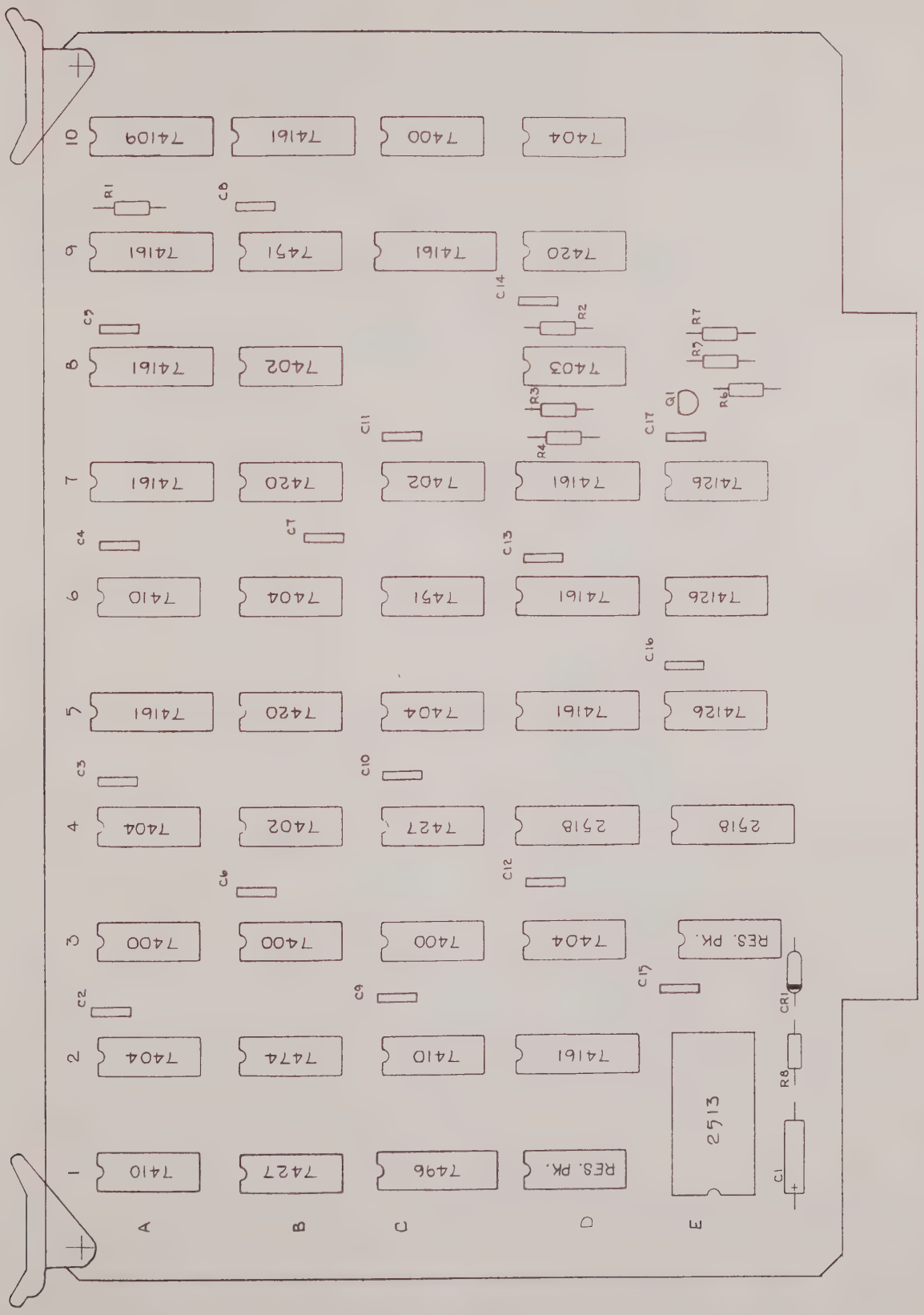
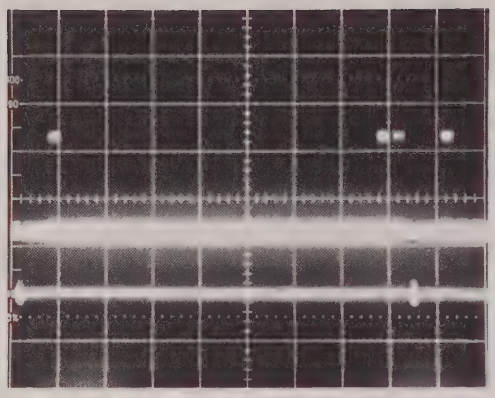
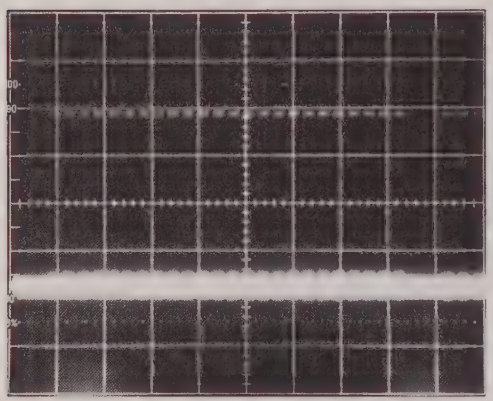


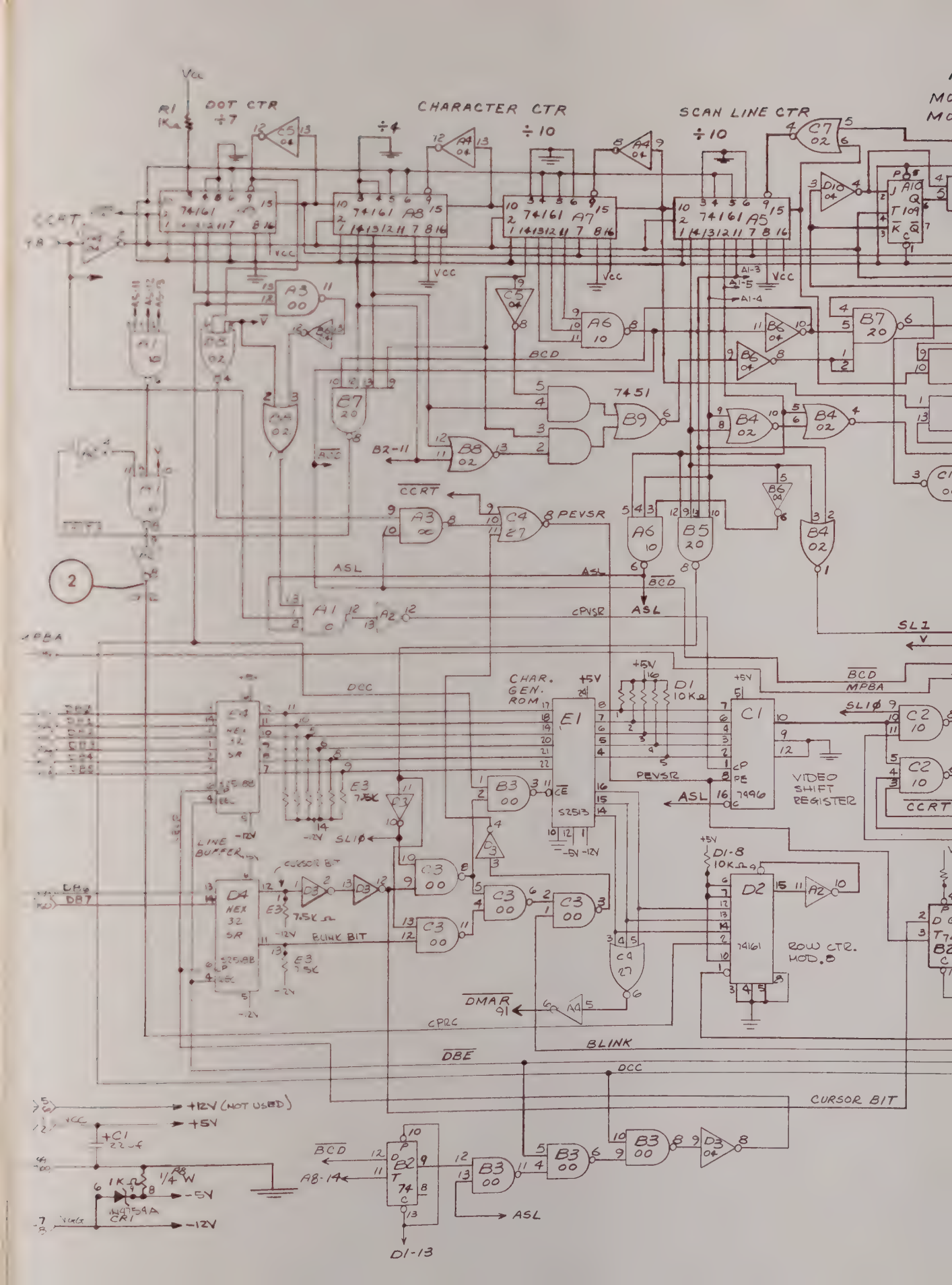

Figure 9.6 CRT Driver Assembly Drawing



1. Vert. 2 msec
   Horiz. 0.5V
   Ext. Trig. A10-10 (+)
   Output Q1 at R6



2. Vert. 1V
   Horiz. 2 msec
   Ext. Trig. A10-10 (+)


DOT CTR ÷7
CHARACTER CTR ÷10
SCAN LINE CTR ÷10
÷4
R1 1K
74161 A8
74161 A7
74161 A5
BCD
7451 B9
B2-11
CCRT
PEVSR
ASL
CPVSR
SL1
CHAR. GEN. ROM E1
S2513
D1 10KΩ
C1 7496
VIDEO SHIFT REGISTER
C2 10
LINE BUFFER
CURSOR BIT
BLINK BIT
E3 7.5K
D4 NEX 32 SR
D2 74161
ROW CTR. MOD.9
DMAR
CPRC
BLINK
DBE
DCC
CURSOR BIT
+12V (NOT USED)
+5V
-5V
-12V
+C1 22μf
1K R8 1/4W
1N4754A CR1
B2 74
D1-13

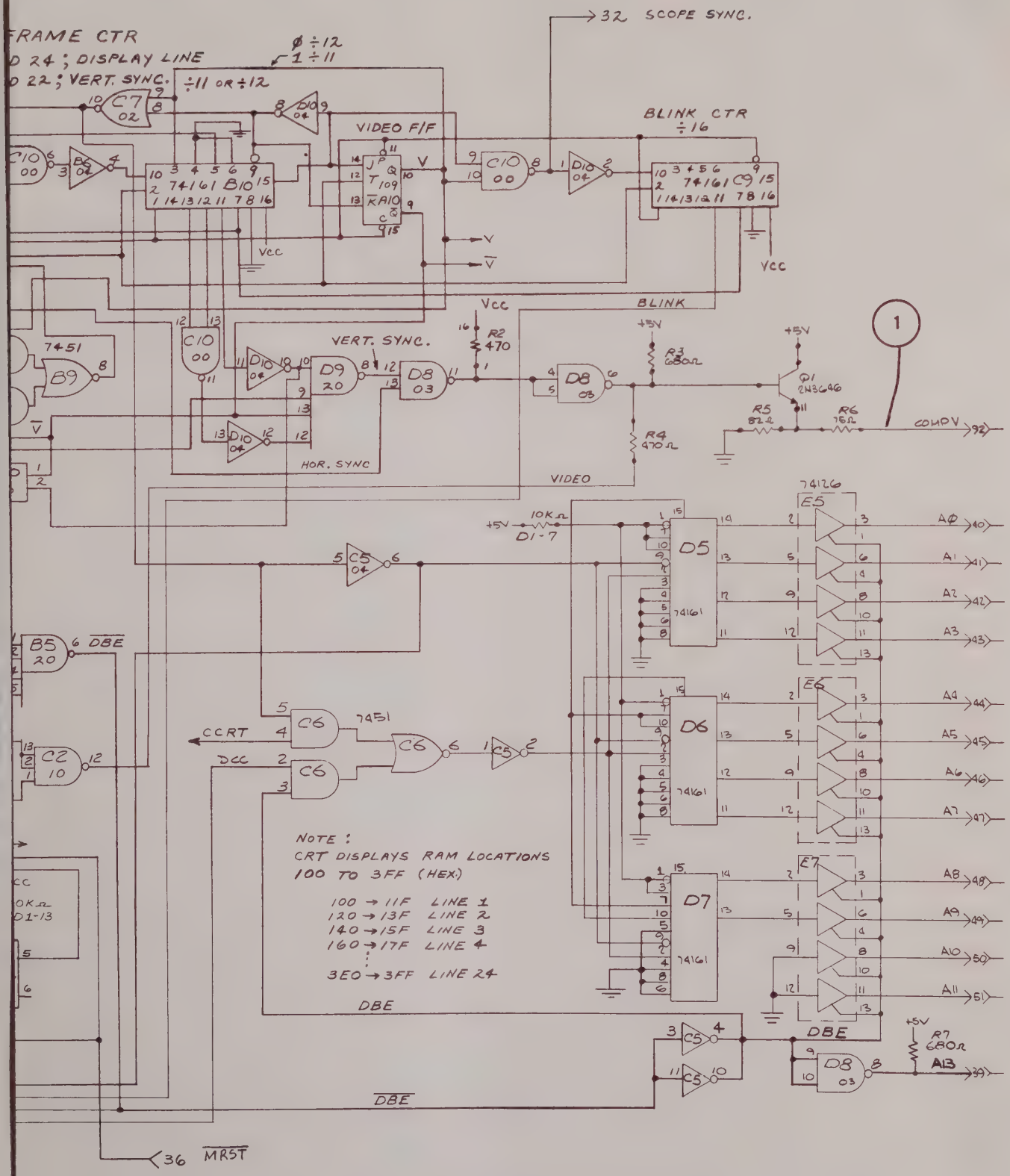



Figure 9.7 CRT Driver Schematic

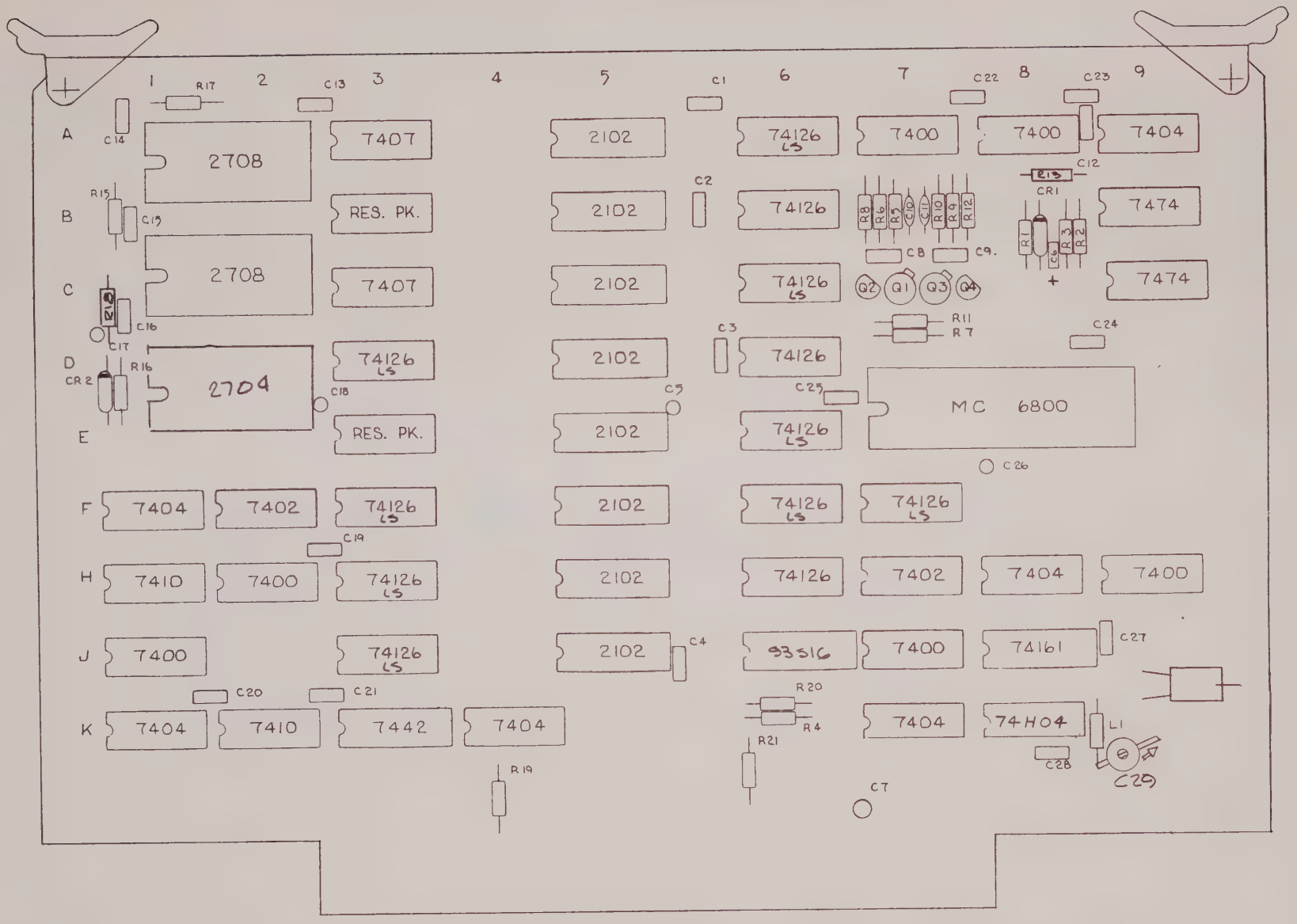



Figure 9.8 MPU Assembly Drawing

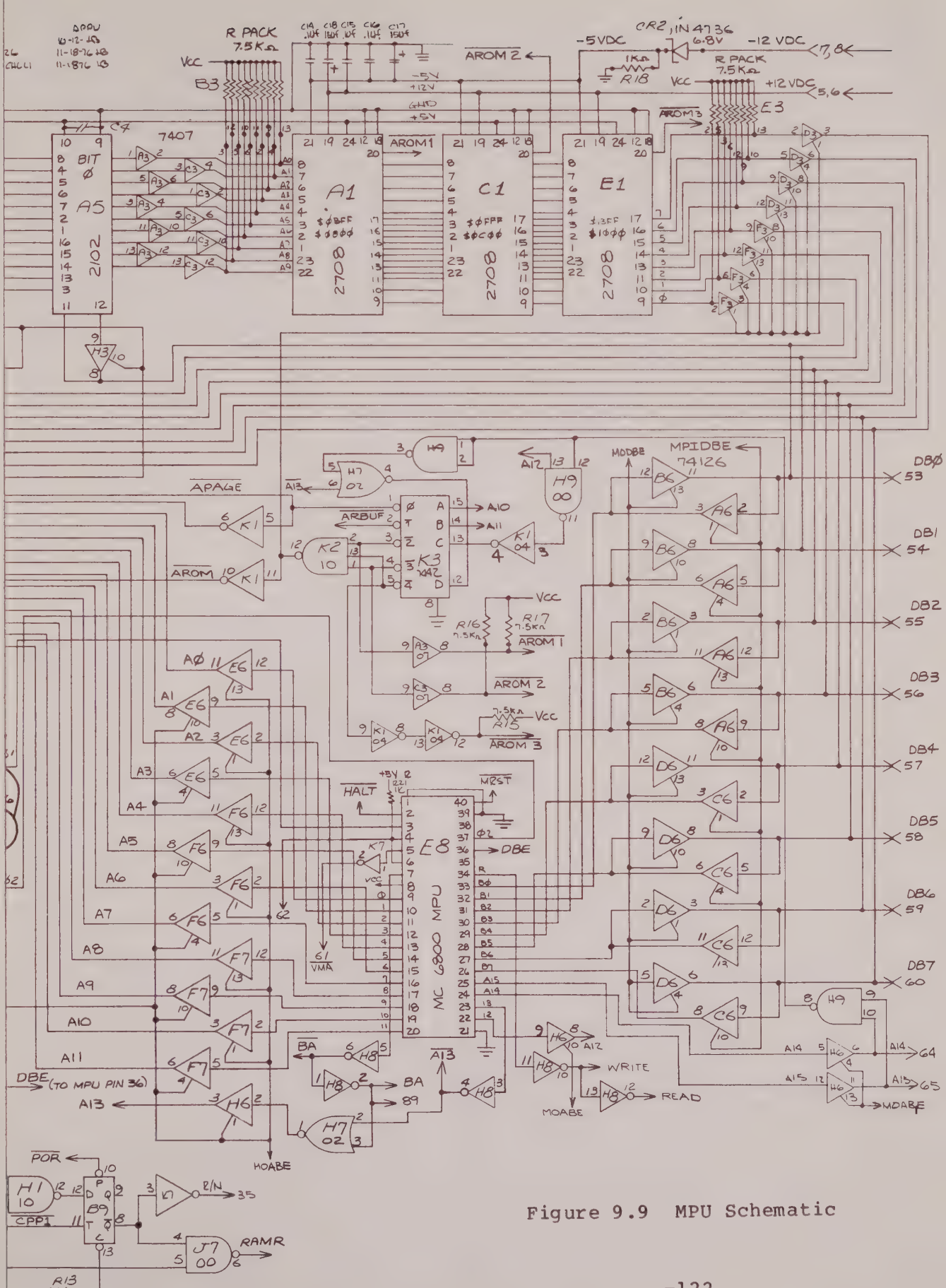
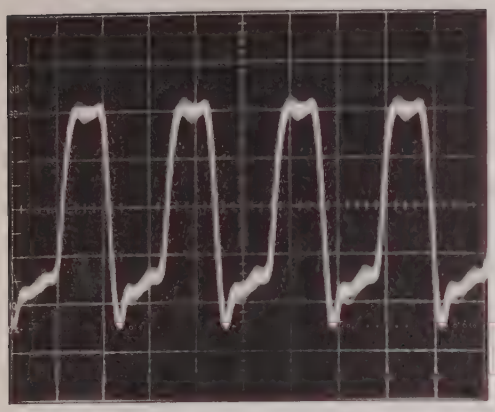
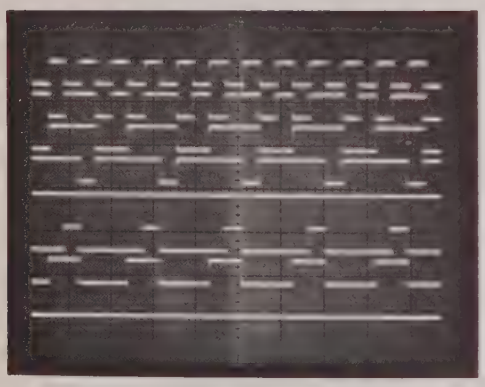



Figure 9.9 MPU Schematic

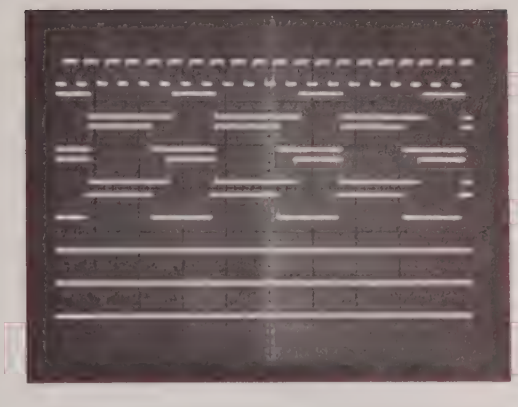


1. Vert. 1 V
   Horiz. 0.02 μsec
   Int. Trig. (+)



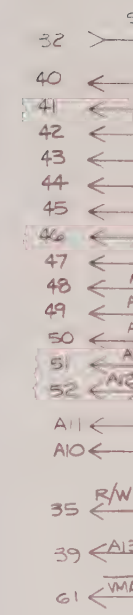
2.

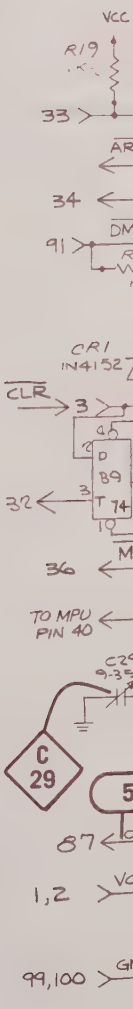
| *Probes* | *851-D Settings* |
|---|---|
| 1. J6-2 | Trig. Source—I(T) |
| 2. J6-14 | Record Mode—Pretrig. |
| 3. J6-13 | Input—Latch |
| 4. J6-12 | Delay—40 |
| 5. J6-11 | Trig. on CH 2 |
| 6. J6-15 | CH 1-4—TTL |
| 7. K7-10 | CH 5-8—TTL |
| 8. NC | Clk Rate—Ext. J6-2 |
| | Clk Source—Ext. (+) |
| | Horiz.—X20 |
| | Display—MX |

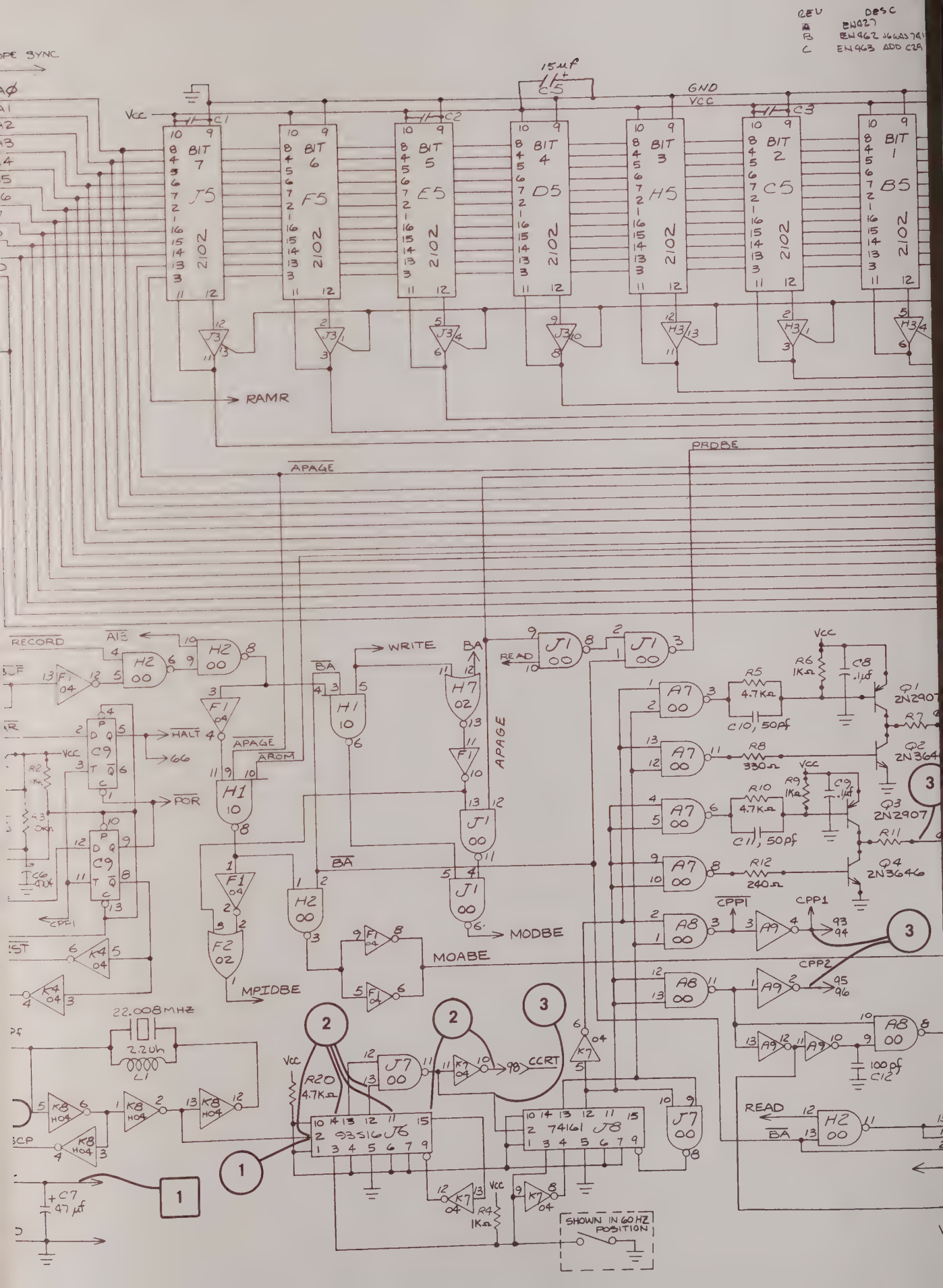


3.

| *Probes* | *851-D Settings* |
|---|---|
| 1. J8-2 | Trig. Source—I(T) |
| 2. A9-4 | Record Mode—Pretrig. |
| 3. A9-2 | Input—Latch |
| 4. R7 | Delay—40 |
| 5. R11 | Trig. on CH 1 |
| 6. NC | CH 1-4—TTL |
| 7. NC | CH 5-8—TTL |
| 8. NC | Clk Rate—22.008 MHz |
| | Clk Source—Ext. (+) |
| | Horiz.—X5 |
| | Display—EX |




REV DESC
A EN927
B EN962 J6&J8 74161
C EN963 ADD C29
15µF
C5
GND
VCC
Vcc
C1
C2
C3
8 BIT 7 J5 2102
8 BIT 6 F5 2102
8 BIT 5 E5 2102
8 BIT 4 D5 2102
8 BIT 3 H5 2102
8 BIT 2 C5 2102
8 BIT 1 B5 2102
RAMR
APAGE
PRDBE
RECORD
WRITE
READ
BA
HALT
POR
AROM
MODBE
MOABE
MPIDBE
CPP1
CPP2
CCRT
22.008MHZ
2.2uh
L1
+C7 47 µf
R20 4.7KΩ
R4 1KΩ
R5 4.7KΩ
C10, 50pf
R6 1KΩ
C8 .1µf
Q1 2N2907
R7
R8 330Ω
Q2 2N3646
R9 1KΩ
C9 .1µf
R10 4.7KΩ
C11, 50pf
Q3 2N2907
R11
R12 240Ω
Q4 2N3646
100pf C12
SHOWN IN 60HZ POSITION
93516 J6
74161 J8

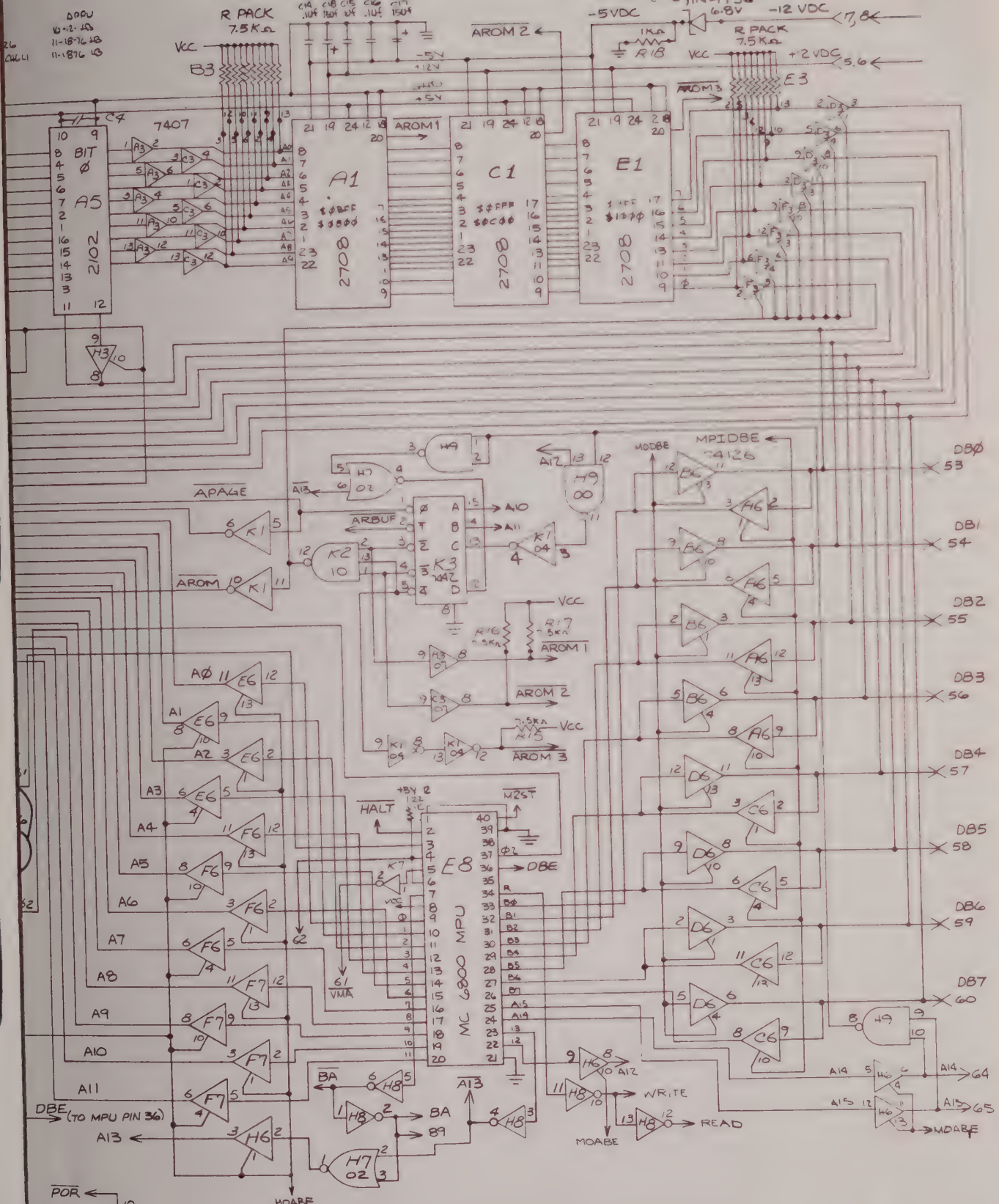



Figure 9.9 MPU Schematic

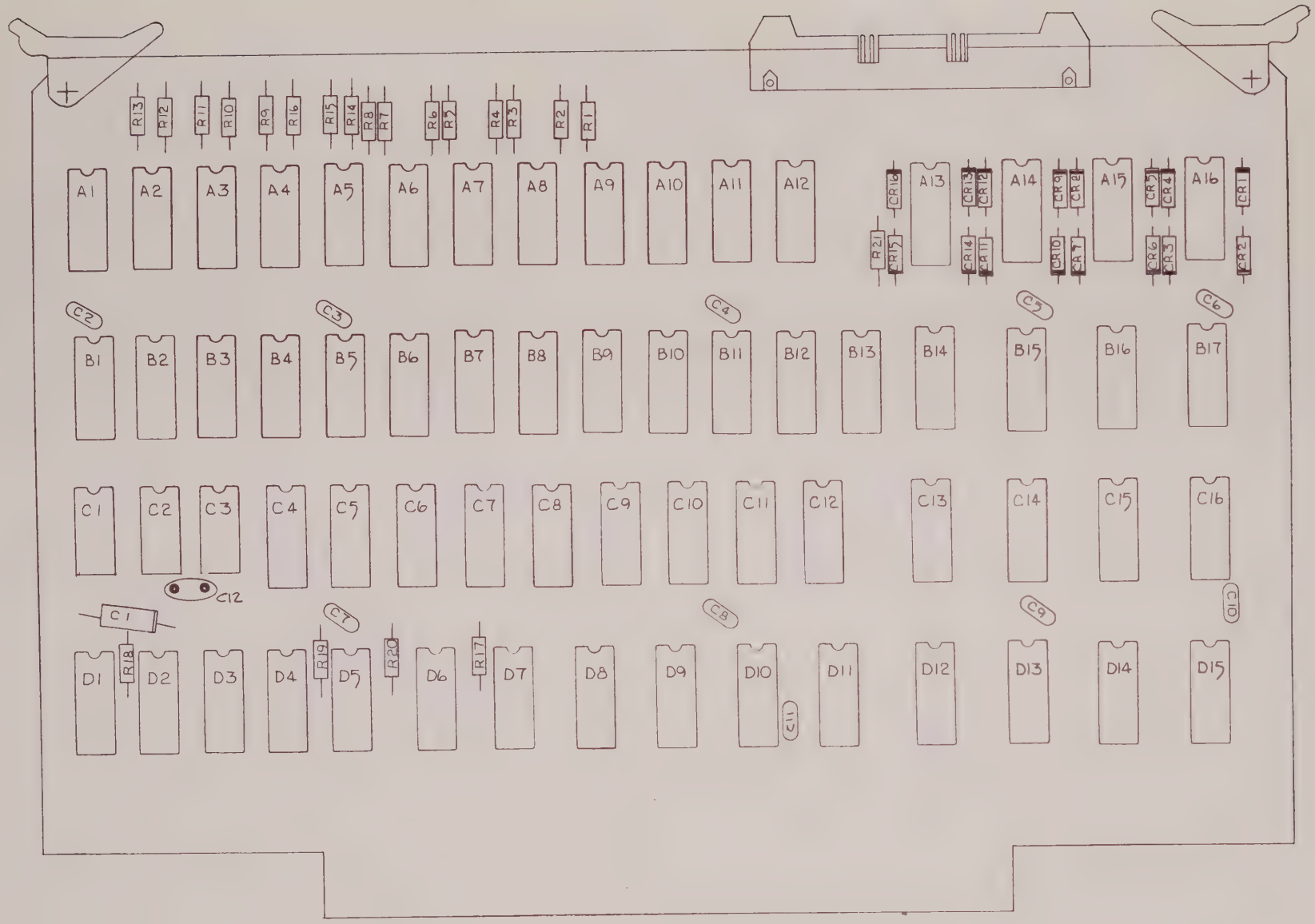



Figure 9.10 Record Assembly Drawing

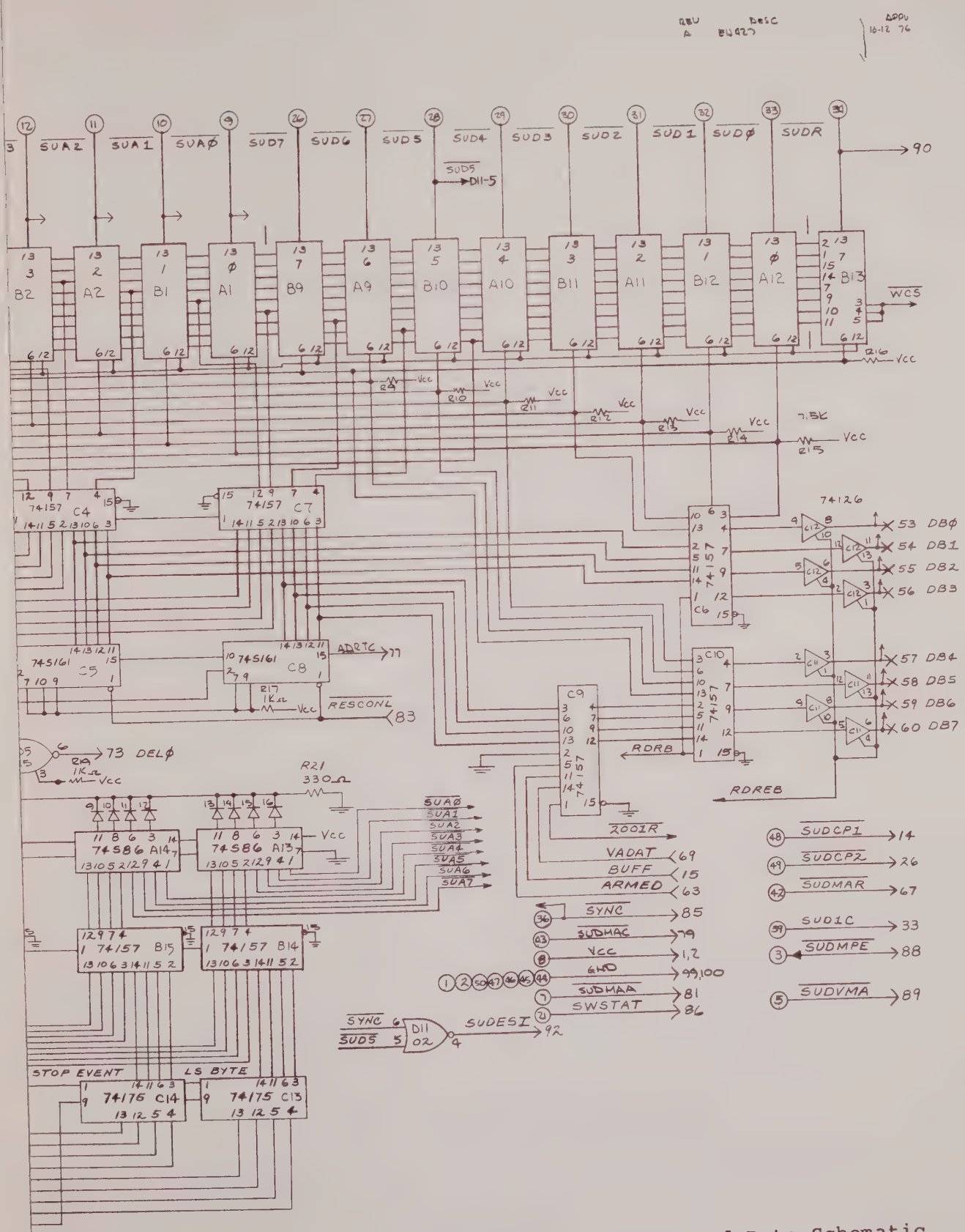
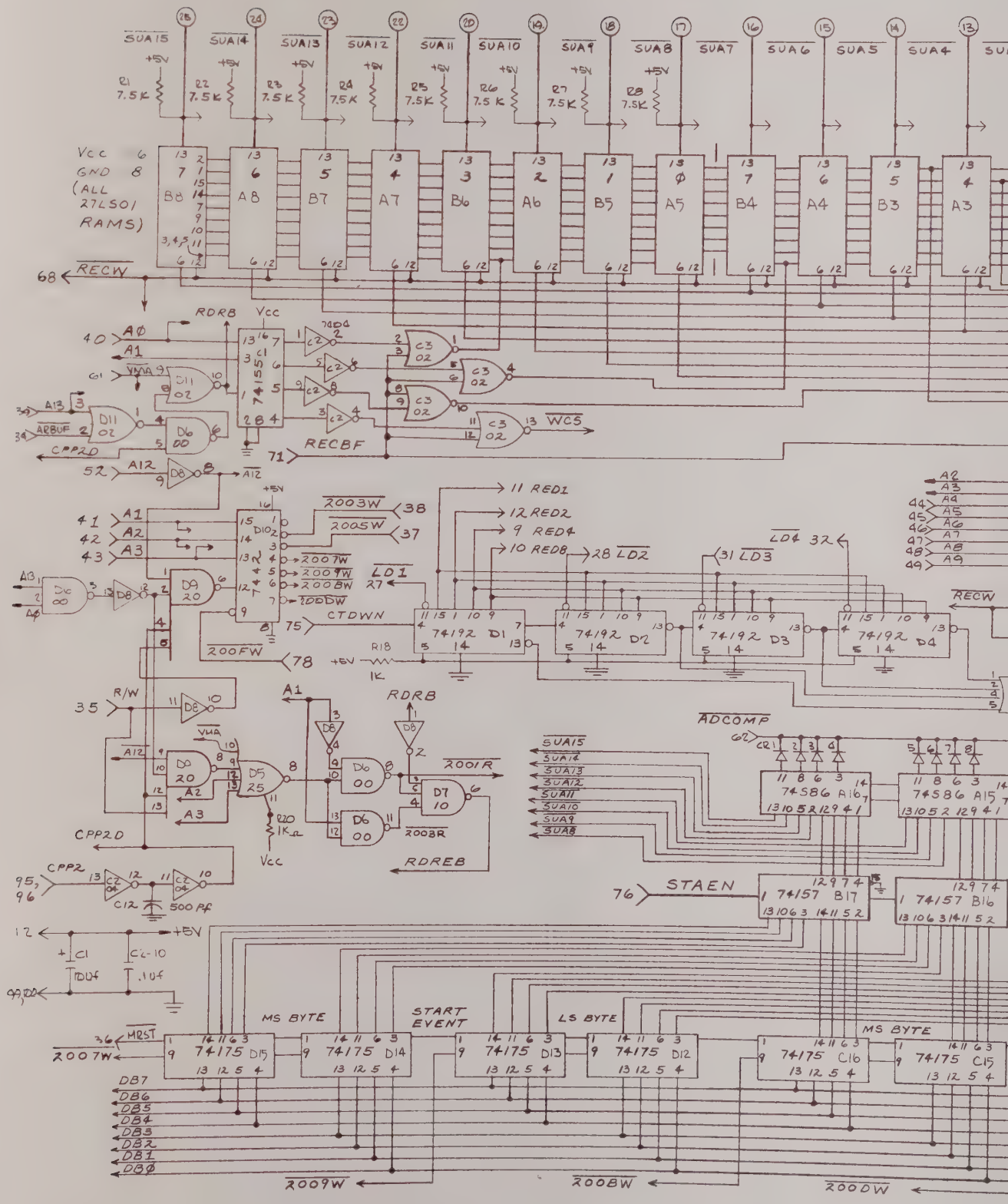



Figure 9.11 Record Data Schematic


SUA15
SUA14
SUA13
SUA12
SUA11
SUA10
SUA9
SUA8
SUA7
SUA6
SUA5
SUA4
R1 7.5K
R2 7.5K
R3 7.5K
R4 7.5K
R5 7.5K
R6 7.5K
R7 7.5K
R8 7.5K
+5V
Vcc 6
GND 8
(ALL 27LS01 RAMS)
B8
A8
B7
A7
B6
A6
B5
A5
B4
A4
B3
A3
68 RECW
RDRB
Vcc
40 A0
A1
A13
ARBUF
CPP2D
52 A12
71 RECBF
WC5
41 A1
42 A2
43 A3
2003W
2005W
2007W
2009W
200BW
200DW
LD1
27
CTDWN
75
200FW
78
R18 1K
11 RED1
12 RED2
9 RED4
10 RED8
28 LD2
31 LD3
LD4 32
74192 D1
74192 D2
74192 D3
74192 D4
RECW
A2
A3
A4
A5
A6
A7
A8
A9
44
45
46
47
48
49
R/W
35
VMA
A12
A1
A2
A3
RDRB
2001R
2003R
RDREB
R20 1K
Vcc
CPP2D
CPP2
95, 96
C12 500 pf
ADCOMP
62
74S86 A16
74S86 A15
SUA15
SUA14
SUA13
SUA12
SUA11
SUA10
SUA9
SUA8
76 STAEN
74157 B17
74157 B16
12 +5V
C1 100f
C2-10 .10f
99,100
MS BYTE
START EVENT
LS BYTE
MS BYTE
36 MRST
2007W
74175 D15
74175 D14
74175 D13
74175 D12
74175 C16
74175 C15
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0
2009W
200BW
200DW

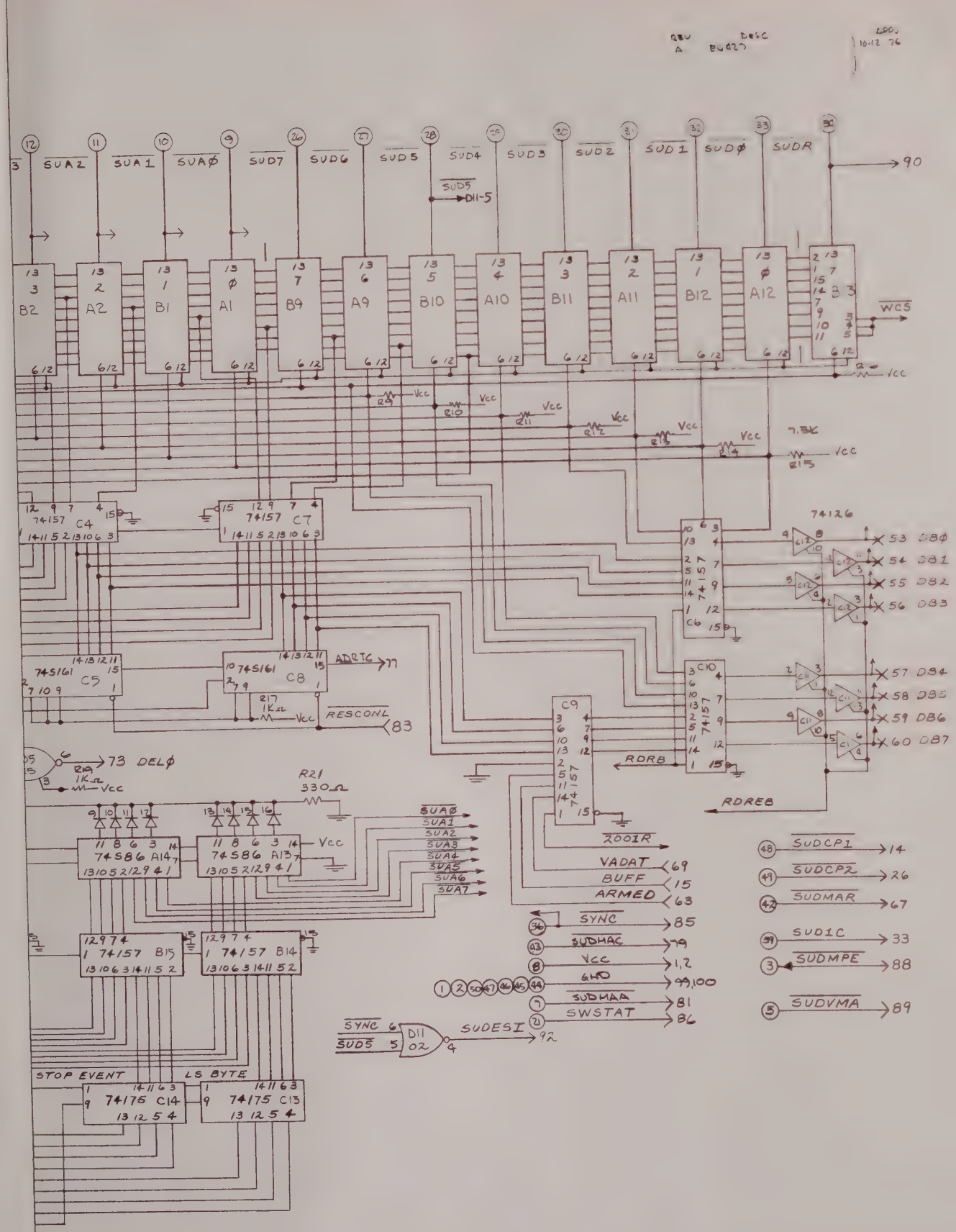



Figure 9.11 Record Data Schematic

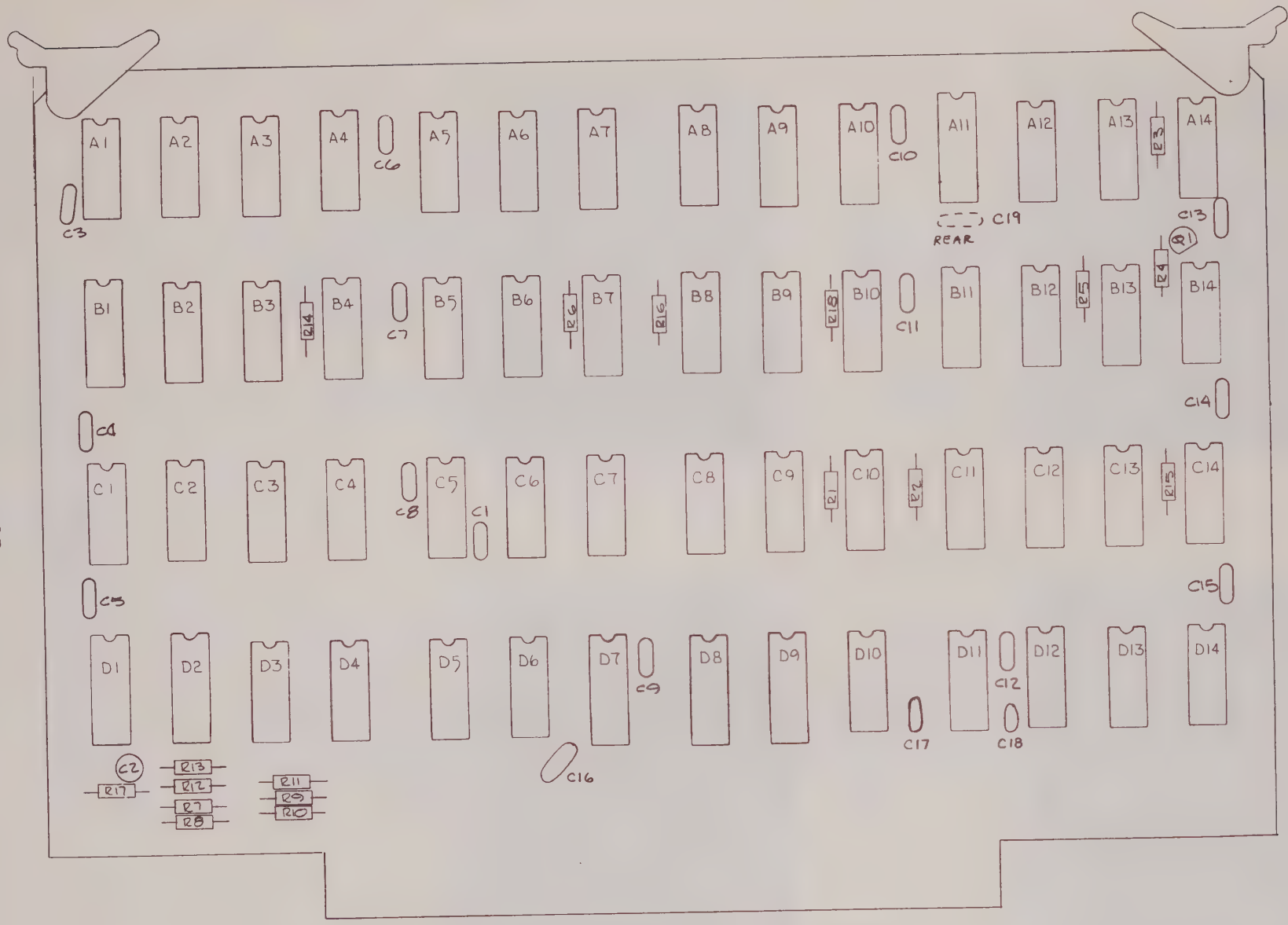
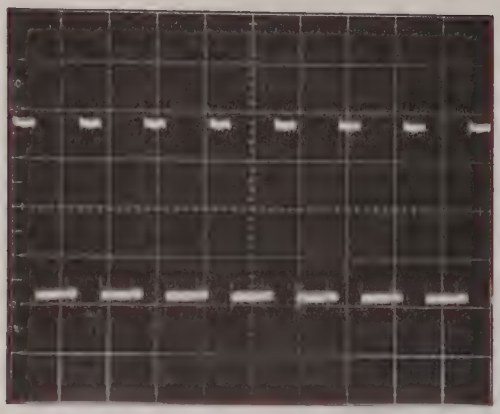
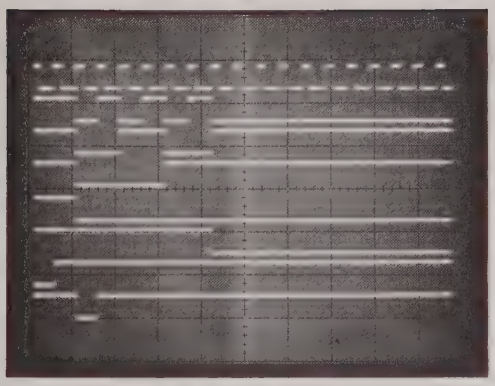



Figure 9.12 Record Control Assembly Drawing

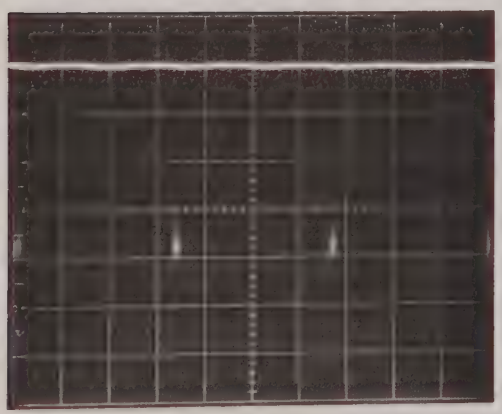


1. Vert. 1 V
Horiz. 1 μsec
Int. Trig. (+)

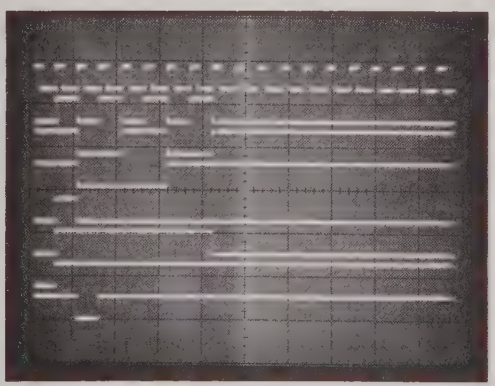


3A.

| *Probes* | *851-D Settings* |
|---|---|
| 1. D1-2 | Trig. Source—I(T) |
| 2. D1-14 | Record Mode—Pretrig. |
| 3. D1-13 | Input—Latch |
| 4. D1-12 | Pretrig. Mem. Delay—50 |
| 5. D1-11 | Trig.—CH 2 |
| 6. D1-7 & 10 | CH 1-4—A |
| 7. D1-9 | CH 5-8—A |
| 8. D2-1 | Int Clk—0.05 μsec |
| | Clk Source—Int. |
| | Horiz.—X5 |
| | Display—X1 |



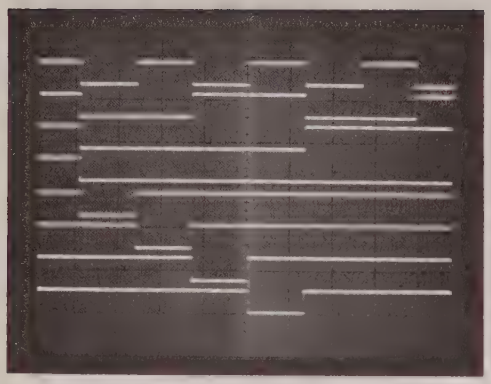
2. Vert. 1 V/cm
Horiz. 5 msec/cm
Int. Trig. (−)



3B.

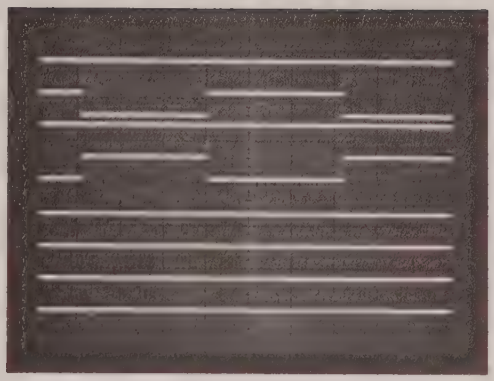
| *Probes* | *851-D Settings* |
|---|---|
| 1. D1-2 | Trig. Source—I(T) |
| 2. D1-14 | Record Mode—Pretrig. |
| 3. D1-13 | Input—Latch |
| 4. D1-12 | Pretrig. Mem. Delay—50 |
| 5. D1-11 | Trig.—CH 2 |
| 6. D1-7 & 10 | CH 1-4—A |
| 7. D1-9 | CH 5-8—A |
| 8. D2-1 | Int Clk—0.05 μsec |
| | Clk Source—Int. |
| | Horiz.—X5 |
| | Display—X1 |

Figure 9.13 Waveform Photographs to the Record Control Board



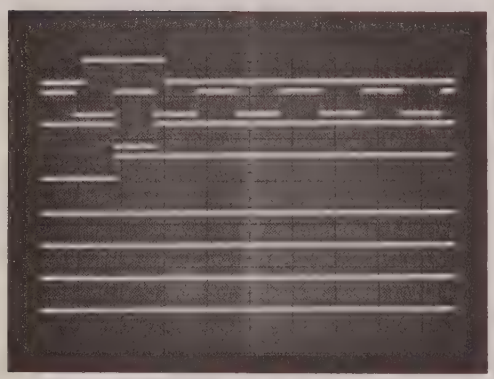
4.

| *Probes* | *851-D Settings* |
|---|---|
| 1. D2-15 | Trig. Source—I(T) |
| 2. D2-14 | Record Mode—Pretrig. |
| 3. D2-13 | Input—Latch |
| 4. D2-12 | Delay—50 |
| 5. D2-1 | Trig. on CH 1 |
| 6. D2-2 | CH 1-4—A |
| 7. D3-3 | CH 5-8—A |
| 8. D3-4 | Clk Rate—0.02 μsec. |
| | Clk Source—Int. |
| | Horiz.—X5 |
| | Display—X1 |



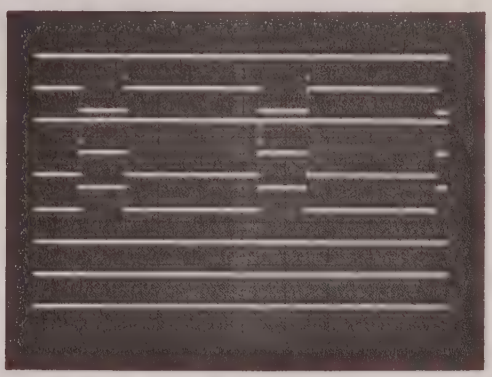
6.

| *Probes* | *851-D Settings* |
|---|---|
| 1. D4-3 | Trig. Source—I(T) |
| 2. D4-5 | Record Mode—Pretrig. |
| 3. D4-4 | Input—Latch |
| 4. C4-3 | Delay—50 |
| 5. NC | Trig. on CH 2 |
| 6. NC | CH 1-4—A |
| 7. NC | CH 5-8—A |
| 8. NC | Clk Rate—2.0 μsec |
| | Clk Source—Int. |
| | Horiz.—X5 |
| | Display—X1 |



5.

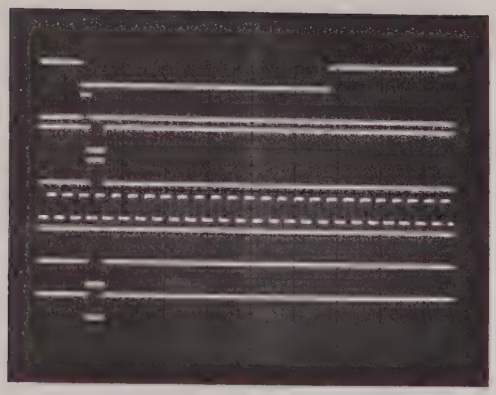
| *Probes* | *851-D Settings* |
|---|---|
| 1. C9-13 | Trig. Source—I(T) |
| 2. C9-12 | Record Mode—Petrig. |
| 3. C9-11 | Input-Latch |
| 4. A6-12 | Delay—150 |
| 5. NC | Trig. on CH 1 |
| 6. NC | CH 1-4—A |
| 7. NC | CH 5-8—A |
| 8. NC | Clk Rate—0.02 μsec. |
| | Clk Source—Int. |
| | Horiz.—X5 |
| | Display—X1 |



7.

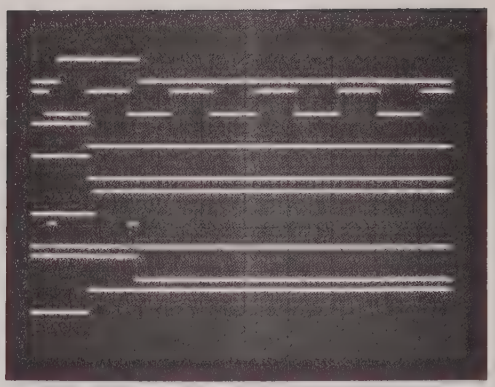
| *Probes* | *851-D Settings* |
|---|---|
| 1. C4-3 | Trig. Source—I(F) |
| 2. C4-5 | Record Mode—Pretrig. |
| 3. C4-1 | Input—Latch |
| 4. A2-6 | Delay—110 |
| 5. A14-9 | Trig. on CH 1 |
| 6. NC | CH 1-4—A |
| 7. NC | CH 5-8—A |
| 8. NC | Clk Rate—5 msec |
| | Clk Source—Int. |
| | Horiz.—X5 |
| | Display—X1 |

Figure 9.13 Waveform Photographs to the Record Control Board



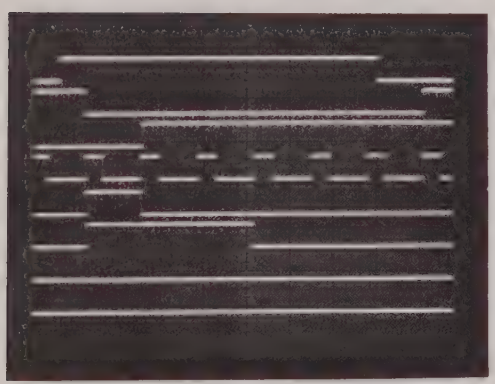
8.

| *Probes* | *851-D Settings* |
|---|---|
| 1. B3-12 | Trig. Source—I(T) |
| 2. B3-3 | Record Mode—Pretrig. |
| 3. B3-13 | Input—Latch |
| 4. B3-5 | Delay—50 |
| 5. B3-9 | Trig. on CH 1 |
| 6. A4-3 | CH 1-4—A |
| 7. A4-6 | CH 5-8—A |
| 8. D5-12 | Clk Rate—0.1 μsec |
| | Clk Source—Int. |
| | Horiz.—X5 |
| | Display—X1 |



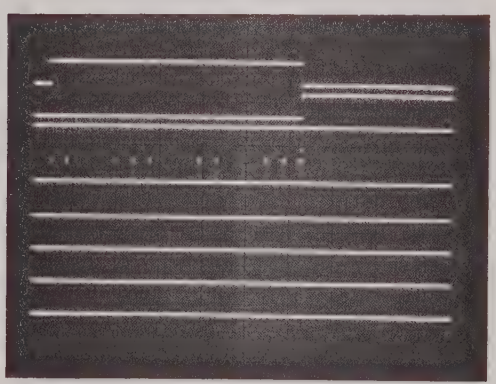
10.

| *Probes* | *851-D Settings* |
|---|---|
| 1. C9-13 | Trig. Source—I(T) |
| 2. C9-12 | Record Mode—Pretrig. |
| 3. A9-12 | Input—Latch |
| 4. A11-10 | Delay—30 |
| 5. A11-9 | Trig. on CH 1 |
| 6. A11-13 | CH 1-4—A |
| 7. A11-5 | CH 5-8—A |
| 8. A6-12 | Clk Rate—0.02 μsec |
| | Clk Source—Int. |
| | Horiz.—X5 |
| | Display—X1 |



9.

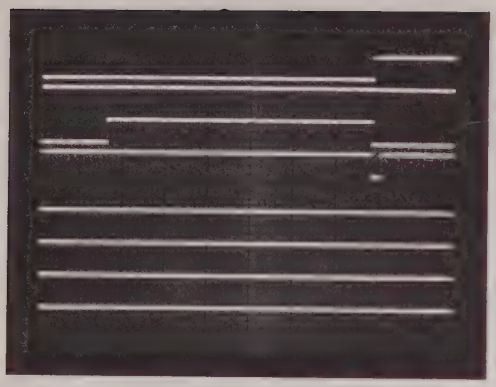
| *Probes* | *851-D Settings* |
|---|---|
| 1. C2-2 | Trig. Source—I(T) |
| 2. C2-6 | Record Mode—Pretrig. |
| 3. C2-9 | Input—Latch |
| 4. C2-3 | Delay—30 |
| 5. B5-4 | Trig. on CH 1 |
| 6. A11-5 | CH 1-4—A |
| 7. NC | CH 5-8—A |
| 8. NC | Clk Rate—0.02 μsec |
| | Clk Source—Int. |
| | Horiz.—X5 |
| | Display—X1 |



11.

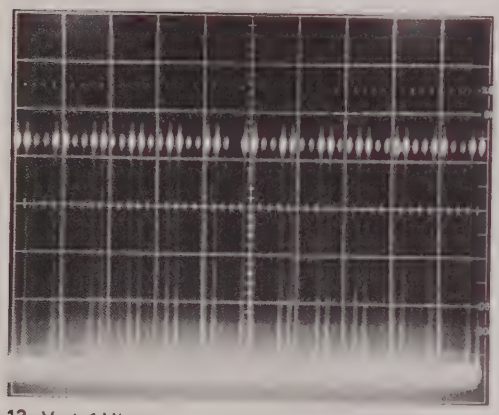
| *Probes* | *851-D Settings* |
|---|---|
| 1. A9-9 | Trig. Source—I(T) |
| 2. A9-10 | Record Mode—Pretrig. |
| 3. A9-8 | Input—Latch |
| 4. D13-11 | Delay—20 |
| 5. NC | Trig. on CH 1 |
| 6. NC | CH 1-4—TTL |
| 7. NC | CH 5-8—TTL |
| 8. NC | Clk Rate—0.1 μsec |
| | Clk Source—Int. |
| | Horiz.—X5 |
| | Display—X1 |

Figure 9.13 Waveform Photographs to the Record Control Board

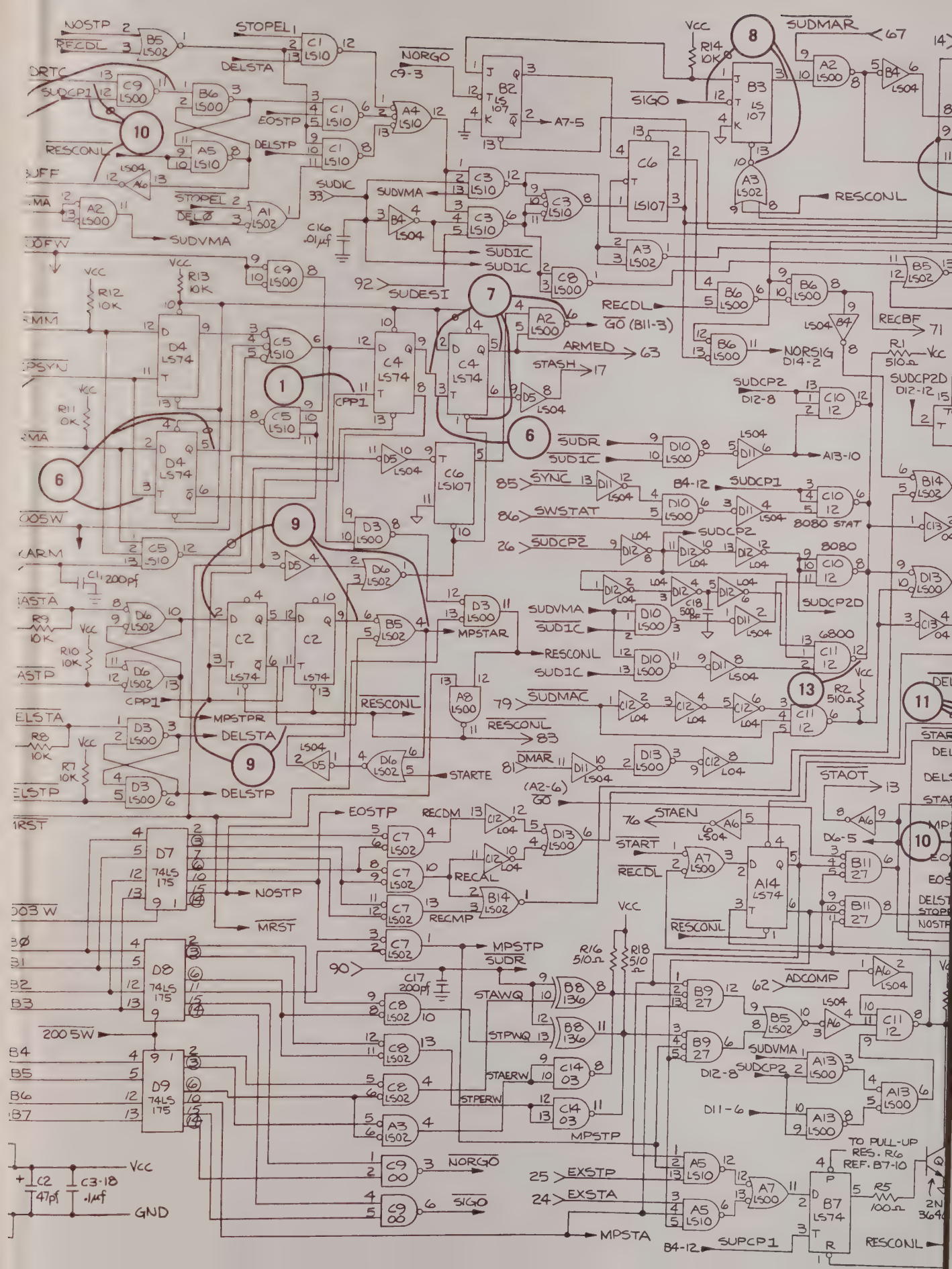


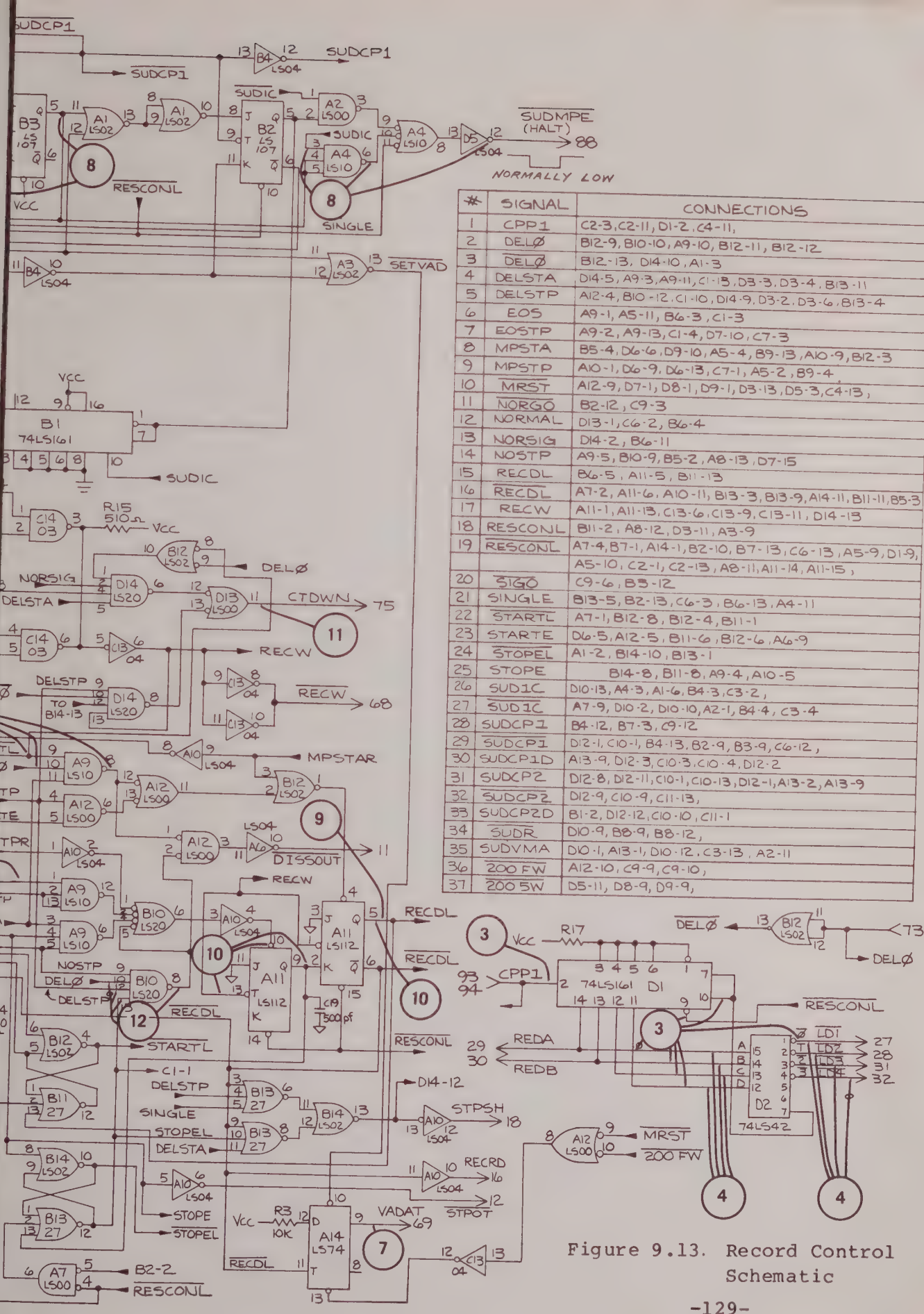
12.

| *Probes* | *851-D Settings* |
|---|---|
| 1. B10-10 | Trig. Source—I(T) |
| 2. B10-12 | Record Mode—Pretrig. |
| 3. B10-13 | Input—Latch |
| 4. B10-8 | Delay—40 |
| 5. NC | Trig.on CH 1 |
| 6. NC | CH 1-4—TTL |
| 7. NC | CH 5-8—TTL |
| 8. NC | Clk Rate—1.0 |
| | Clk Source—Int. |
| | Horiz.—X10 |
| | Display—MX |



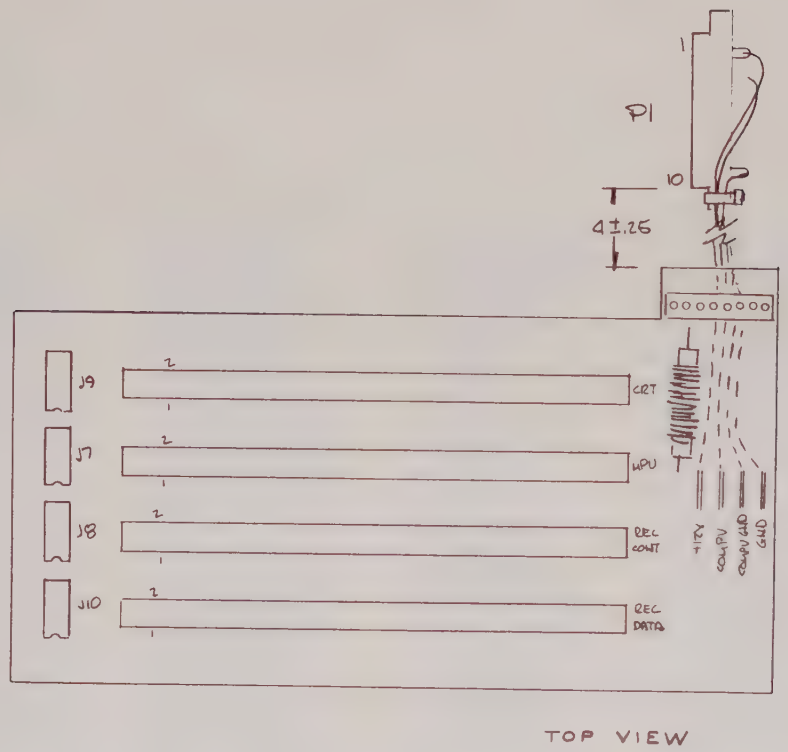
13. Vert. 1 V/cm
Horiz. 5 μsec/cm
Int. Trig. (−)


NOSTP
RECDL
B5 LS02
STOPEL
C1 LS10
DELSTA
NORGO
C9-3
B2 LS 107
A7-5
SUDMAR
67
VCC
R14 10K
B3 LS 107
SUDCP1
C9 LS00
B6 LS00
EOSTP
A4 LS10
SIGO
A2 LS00
B4 LS04
RESCONL
A5 LS10
DELSTP
A3 LS02
SUDIC
SUDVMA
C3 LS10
C16 .01µf
C6 LS107
SUDESI
92
C8 LS00
RECDL
GO (B11-3)
RECBF
71
R12 10K
R13 10K
D4 LS74
ARMED
63
STASH
17
CPP1
C4 LS74
D5 LS04
NORSIG
D14-2
R1 510Ω
SUDCP2D
D12-12
SUDCP2
D12-8
C10 12
SUDR
D10 LS00
D11 LS04
A13-10
SYNC
85
B4-12
SUDCP1
8080 STAT
SWSTAT
86
R11 0K
C5 LS10
C6 LS107
D3 LS00
C1 200pf
SUDCP2
26
8080
6800
R9 10K
R10 10K
D6 LS02
C2 LS74
B5 LS02
MPSTAR
SUDVMA
SUDIC
C18 500pf
RESCONL
MPSTPR
DELSTA
DELSTP
A8 LS00
79
SUDMAC
C12 L04
C11 12
R2 510Ω
R8 10K
R7 10K
STARTE
81
DMAR
(A2-6) GO
STAOT
13
STAEN
76
A6 LS04
START
A7 LS00
A14 LS74
B11 27
D7 74LS 175
EOSTP
RECDM
RECAL
RECMP
B14 LS02
NOSTP
MRST
D8 74LS 175
MPSTP
SUDR
90
R16 510Ω
R18 510Ω
C17 200pf
STAWQ
STPWQ
B8 1360
ADCOMP
62
B9 27
B5 LS02
C11 12
D9 74LS 175
STAERW
STPERW
C14 03
C4 03
A13 LS00
DI2-8
DI1-6
TO PULL-UP RES. R6 REF. B7-10
R5 100Ω
2N 3640
C9 00
NORGO
SIGO
25
EXSTP
24
EXSTA
A5 LS10
A7 LS00
B7 LS74
MPSTA
B4-12
SUPCP1
RESCONL
C2 47pf
C3-18 .1µf
GND




| # | SIGNAL | CONNECTIONS |
|---|---|---|
| 1 | CPP1 | C2-3, C2-11, D1-2, C4-11, |
| 2 | DELØ | B12-9, B10-10, A9-10, B12-11, B12-12 |
| 3 | $\overline{\text{DELØ}}$ | B12-13, D14-10, A1-3 |
| 4 | DELSTA | D14-5, A9-3, A9-11, C1-13, D3-3, D3-4, B13-11 |
| 5 | DELSTP | A12-4, B10-12, C1-10, D14-9, D3-2, D3-6, B13-4 |
| 6 | EOS | A9-1, A5-11, B6-3, C1-3 |
| 7 | EOSTP | A9-2, A9-13, C1-4, D7-10, C7-3 |
| 8 | MPSTA | B5-4, D6-6, D9-10, A5-4, B9-13, A10-9, B12-3 |
| 9 | MPSTP | A10-1, D6-9, D6-13, C7-1, A5-2, B9-4 |
| 10 | $\overline{\text{MRST}}$ | A12-9, D7-1, D8-1, D9-1, D3-13, D5-3, C4-13, |
| 11 | $\overline{\text{NORGO}}$ | B2-12, C9-3 |
| 12 | NORMAL | D13-1, C6-2, B6-4 |
| 13 | NORSIG | D14-2, B6-11 |
| 14 | NOSTP | A9-5, B10-9, B5-2, A8-13, D7-15 |
| 15 | RECDL | B6-5, A11-5, B11-13 |
| 16 | $\overline{\text{RECDL}}$ | A7-2, A11-6, A10-11, B13-3, B13-9, A14-11, B11-11, B5-3 |
| 17 | RECW | A11-1, A11-13, C13-6, C13-9, C13-11, D14-13 |
| 18 | RESCONL | B11-2, A8-12, D3-11, A3-9 |
| 19 | $\overline{\text{RESCONL}}$ | A7-4, B7-1, A14-1, B2-10, B7-13, C6-13, A5-9, D1-9, A5-10, C2-1, C2-13, A8-11, A11-14, A11-15, |
| 20 | $\overline{\text{SIGO}}$ | C9-6, B5-12 |
| 21 | SINGLE | B13-5, B2-13, C6-3, B6-13, A4-11 |
| 22 | $\overline{\text{STARTL}}$ | A7-1, B12-8, B12-4, B11-1 |
| 23 | STARTE | D6-5, A12-5, B11-6, B12-6, A6-9 |
| 24 | $\overline{\text{STOPEL}}$ | A1-2, B14-10, B13-1 |
| 25 | STOPE | B14-8, B11-8, A9-4, A10-5 |
| 26 | SUD1C | D10-13, A4-3, A1-6, B4-3, C3-2, |
| 27 | $\overline{\text{SUD1C}}$ | A7-9, D10-2, D10-10, A2-1, B4-4, C3-4 |
| 28 | SUDCP1 | B4-12, B7-3, C9-12 |
| 29 | $\overline{\text{SUDCP1}}$ | D12-1, C10-1, B4-13, B2-9, B3-9, C6-12, |
| 30 | SUDCP1D | A13-9, D12-3, C10-3, C10-4, D12-2 |
| 31 | SUDCP2 | D12-8, D12-11, C10-1, C10-13, D12-1, A13-2, A13-9 |
| 32 | $\overline{\text{SUDCP2}}$ | D12-9, C10-9, C11-13, |
| 33 | SUDCP2D | B1-2, D12-12, C10-10, C11-1 |
| 34 | $\overline{\text{SUDR}}$ | D10-9, B8-9, B8-12, |
| 35 | SUDVMA | D10-1, A13-1, D10-12, C3-13, A2-11 |
| 36 | $\overline{\text{200 FW}}$ | A12-10, C9-9, C9-10, |
| 37 | $\overline{\text{200 SW}}$ | D5-11, D8-9, D9-9, |

Figure 9.13. Record Control Schematic




| WIRE LIST | | | |
|---|---|---|---|
| FROM | TO | COLOR | |
| P1-1,A | COMPV GND | BLK | } TWIST |
| P1-8,J | COMP V | WHT | |
| P1-7,H | +12V | YEL | |
| P1-10,L | GND | BLK | |

Figure 9.14 Mother Board Assembly Drawing

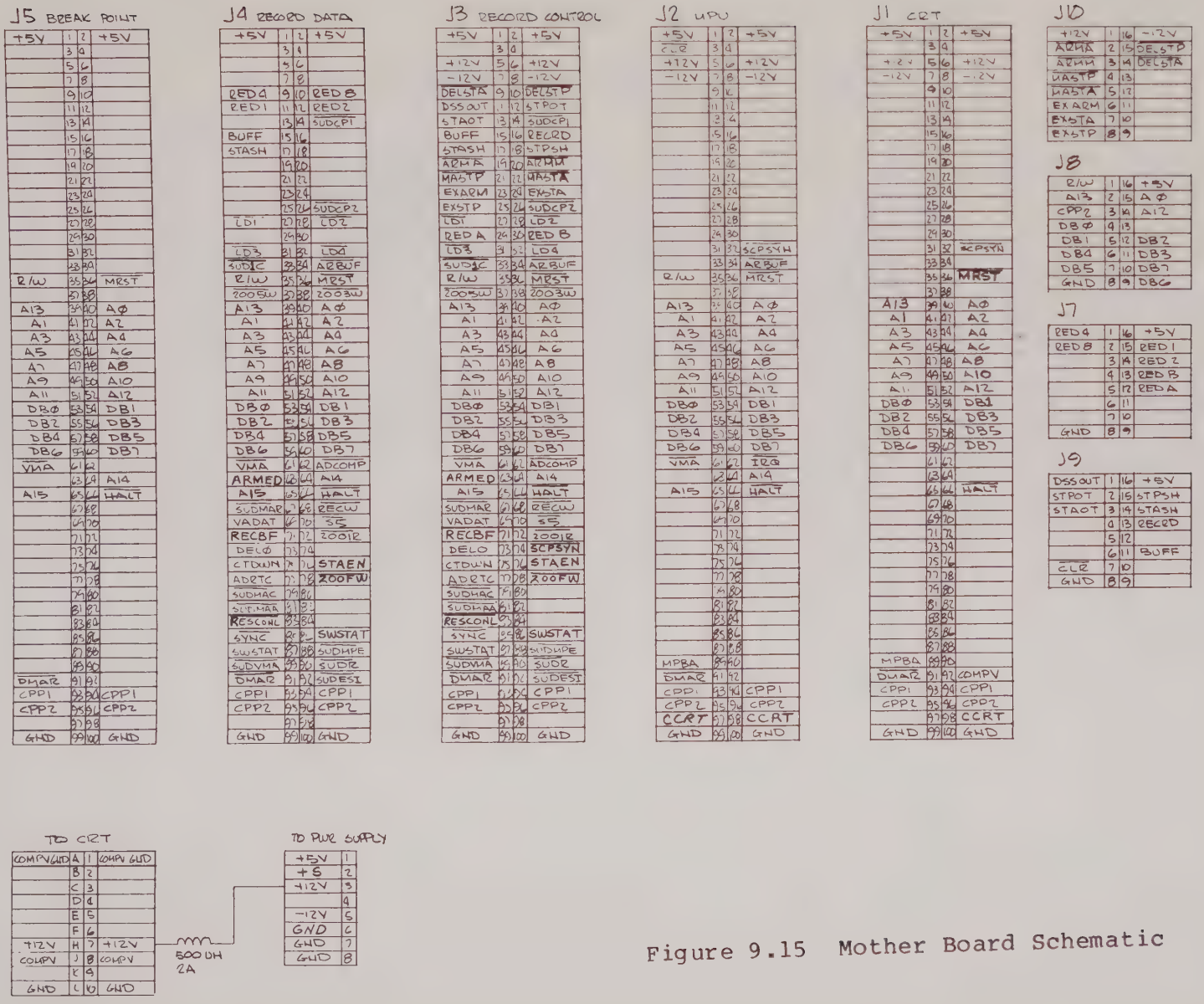



Figure 9.15 Mother Board Schematic

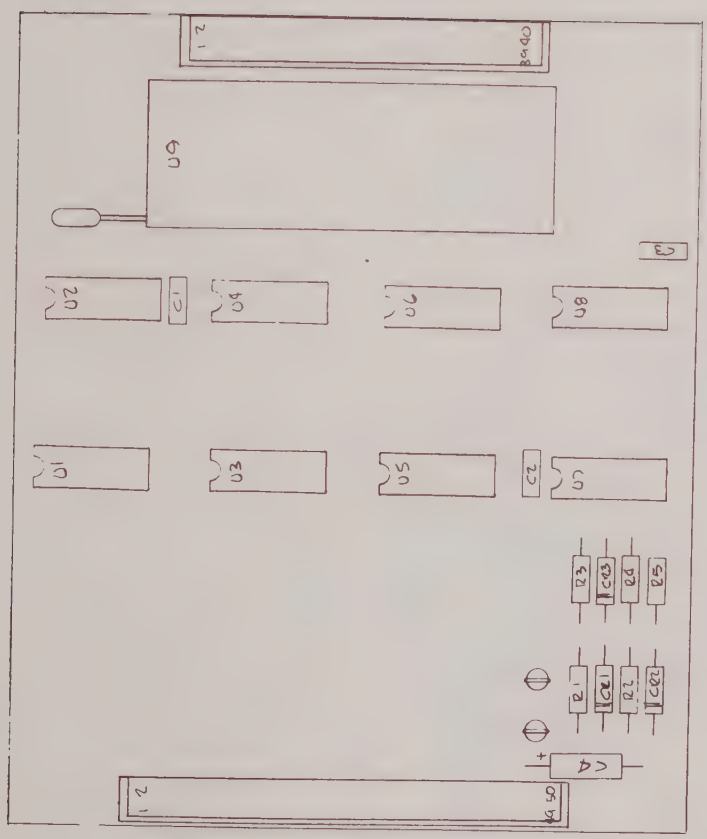



Figure 9.16 6800 Personality Module
Assembly Drawing

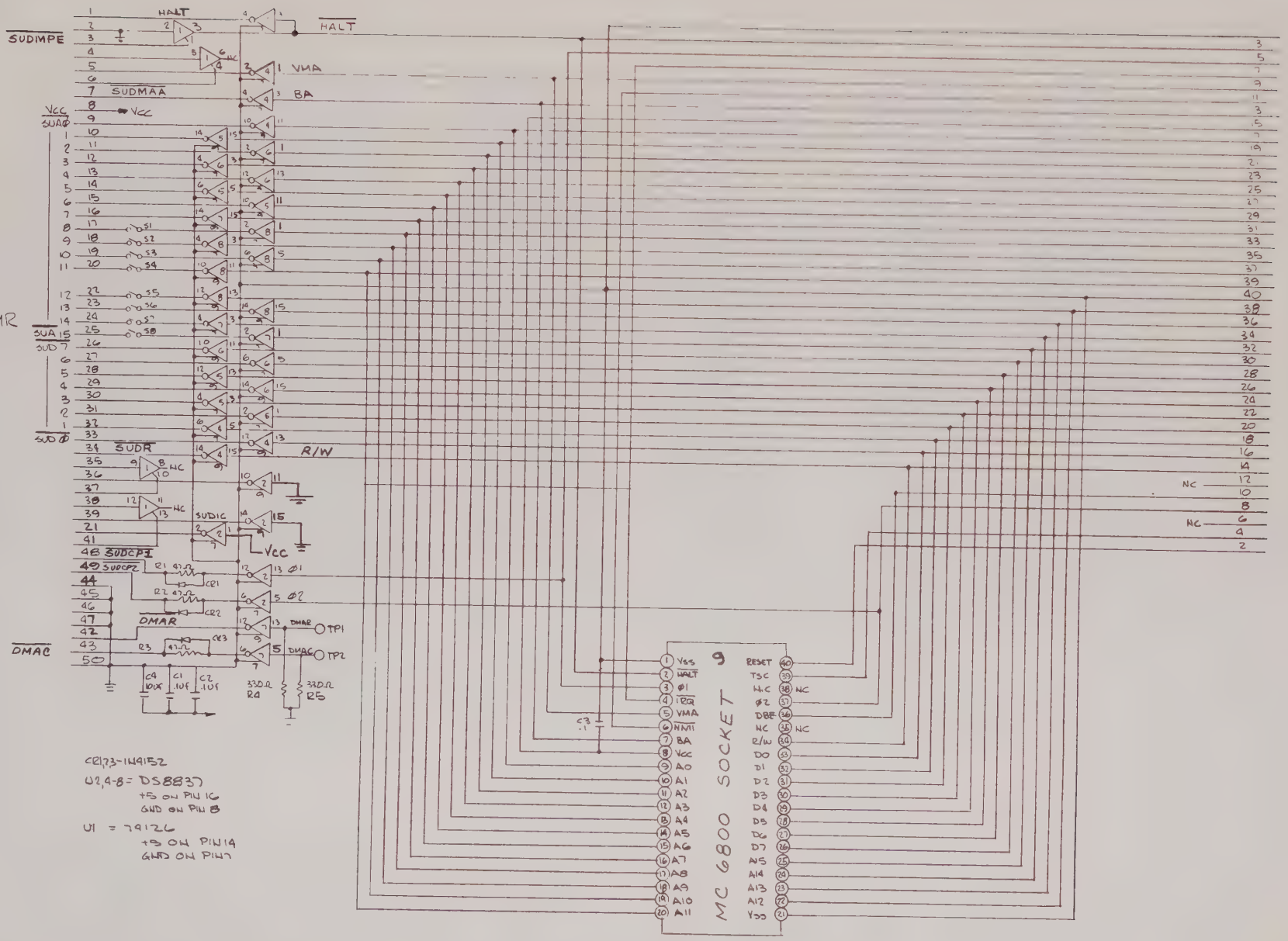



Figure 9.17 6800 Personality Module Schematic

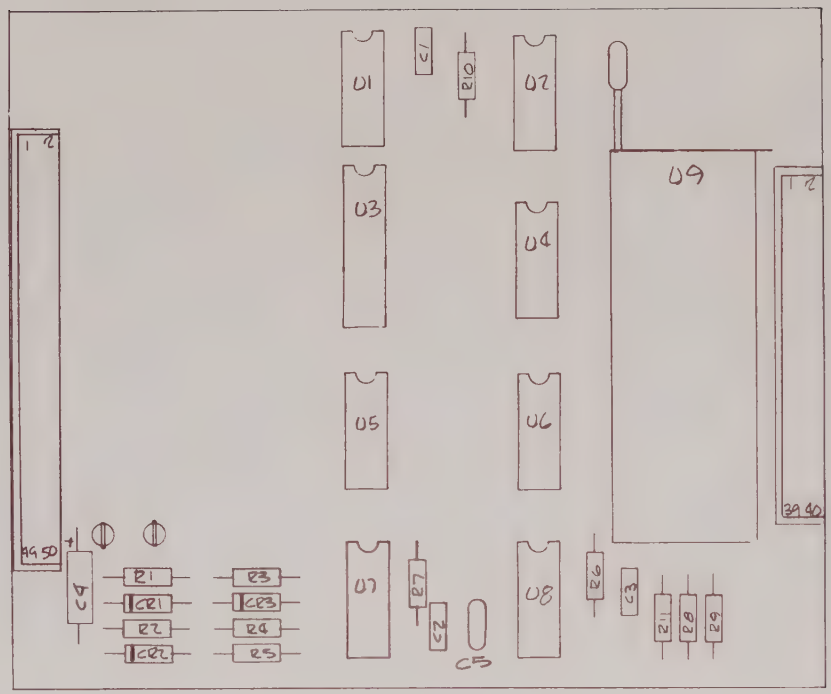



Figure 9.18 8080 Personality Module
Assembly Drawing

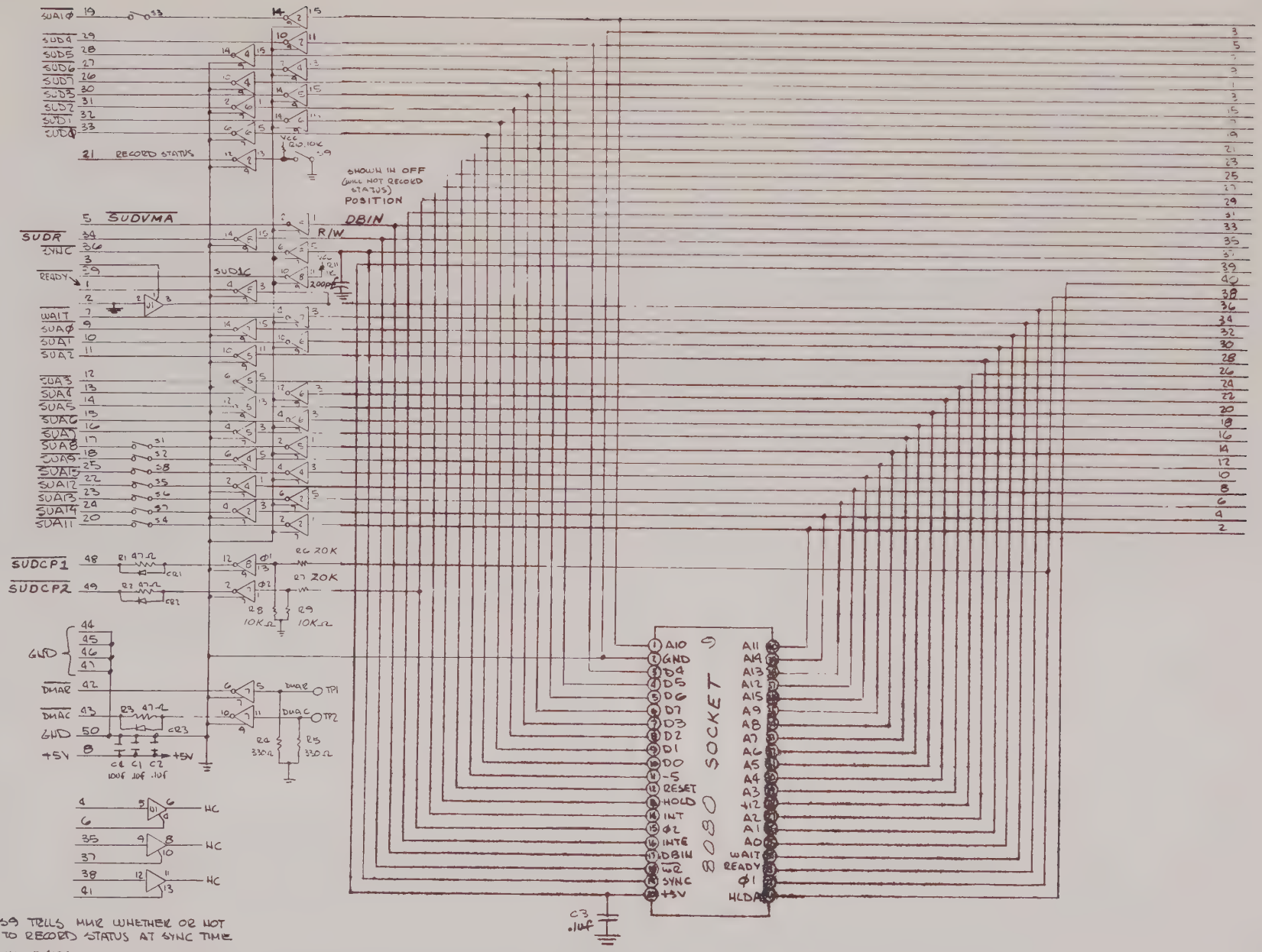



Figure 9.19 8080 Personality Module Schematic

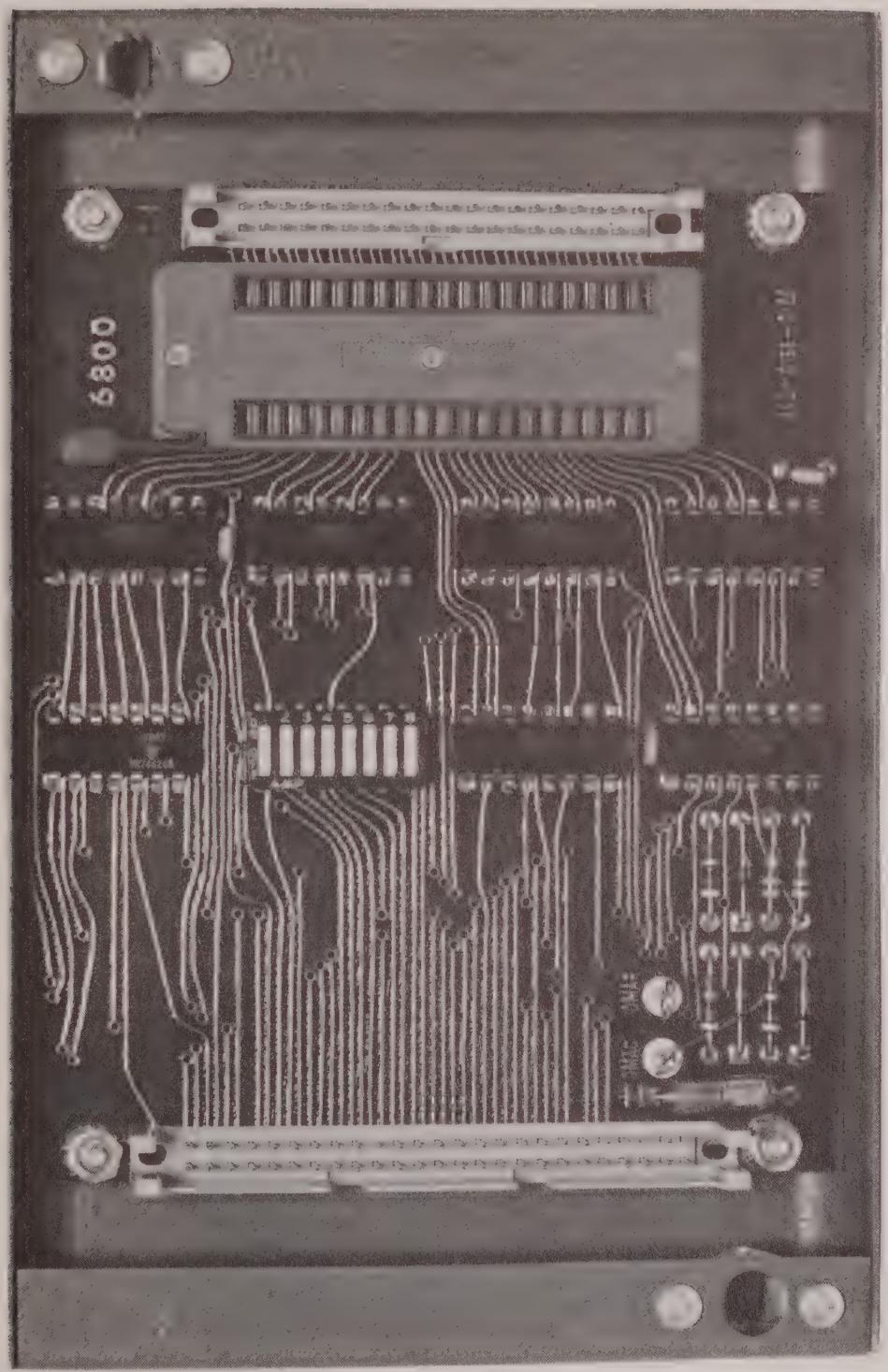
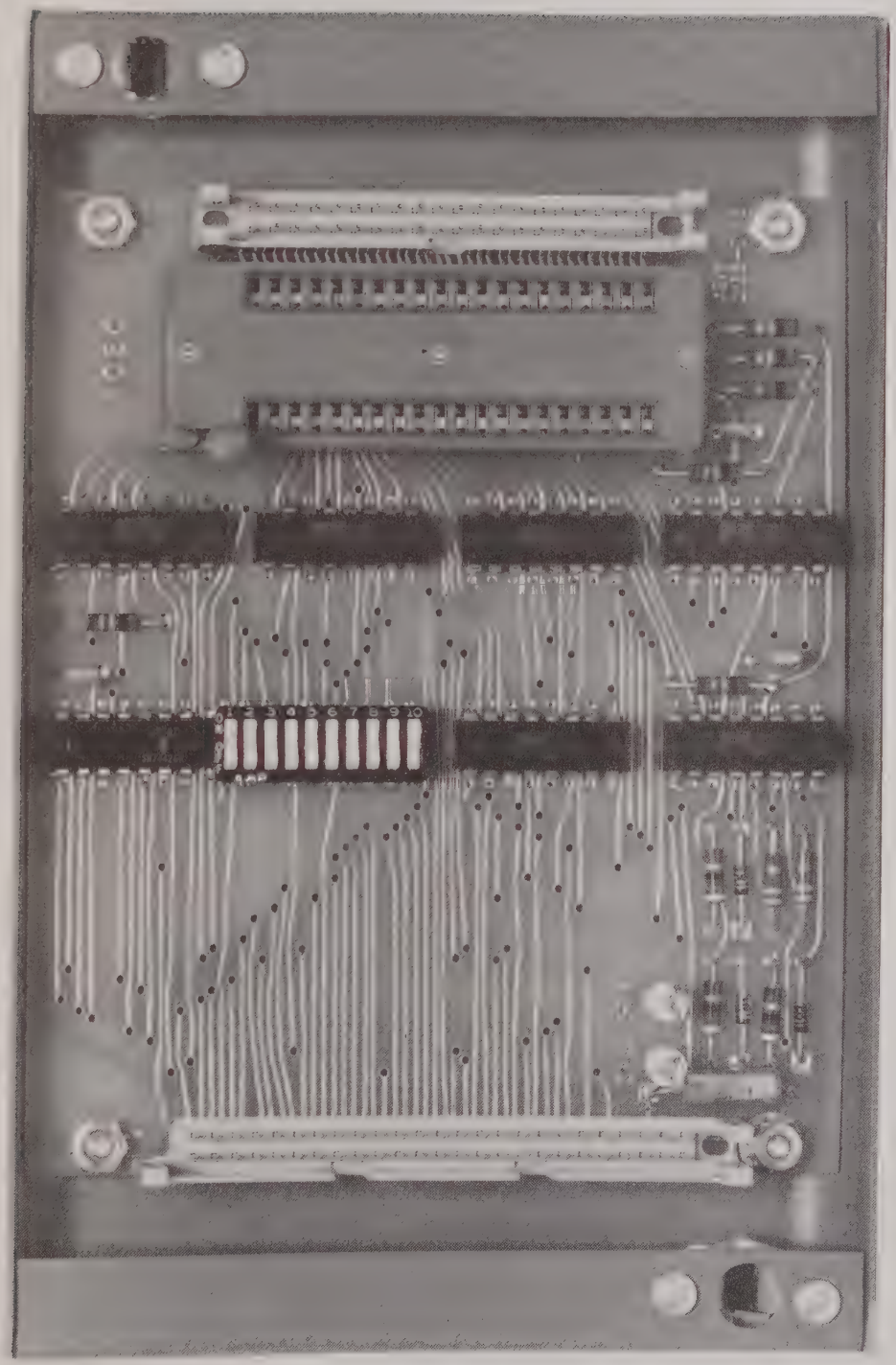



Figure 9.20 6800 Personality Module
Top View



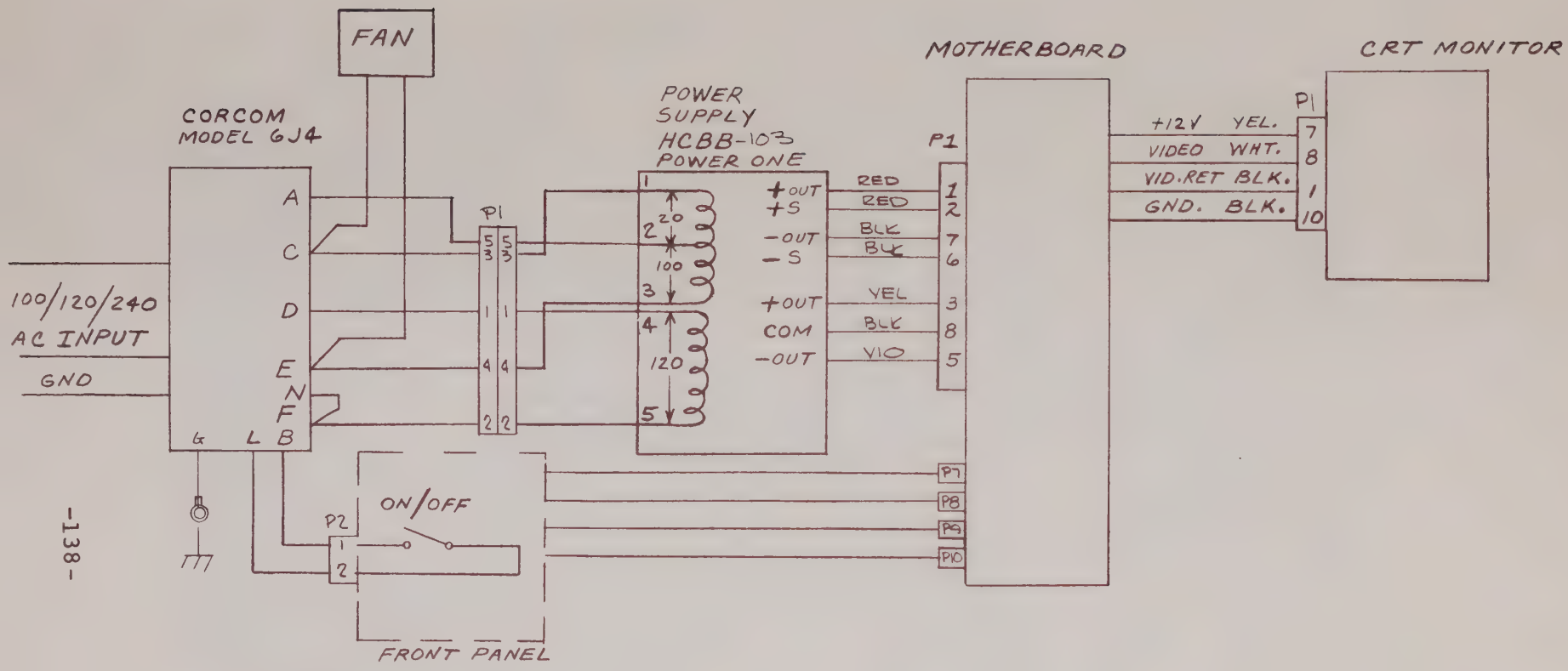
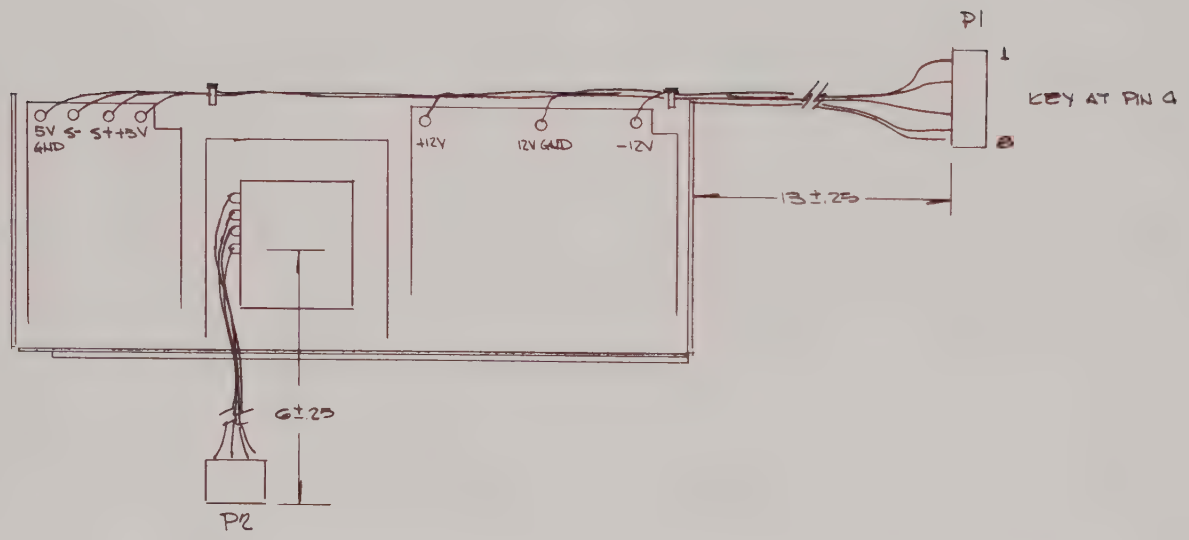



Figure 9.22 System Wiring Schematic




| WIRE LIST | | |
|---|---|---|
| FROM | TO | COLOR |
| P1-1 | +5V | RED |
| P1-3 | +12V | YEL |
| P1-5 | -12V | VIO |
| P1-7 | 5V GND | BLK |
| P1-8 | 12V GND | BLK |
| P2-1 | 4 | VIO |
| P2-2 | 5 | WHT |
| P2-3 | 1 | BLK |
| P2-4 | 3 | RED |
| P1-2 | +S | RED |
| P1-6 | -S | BLK |
| P2-5 | 2 | YEL |

Figure 9.23 Power Supply Assembly Drawings

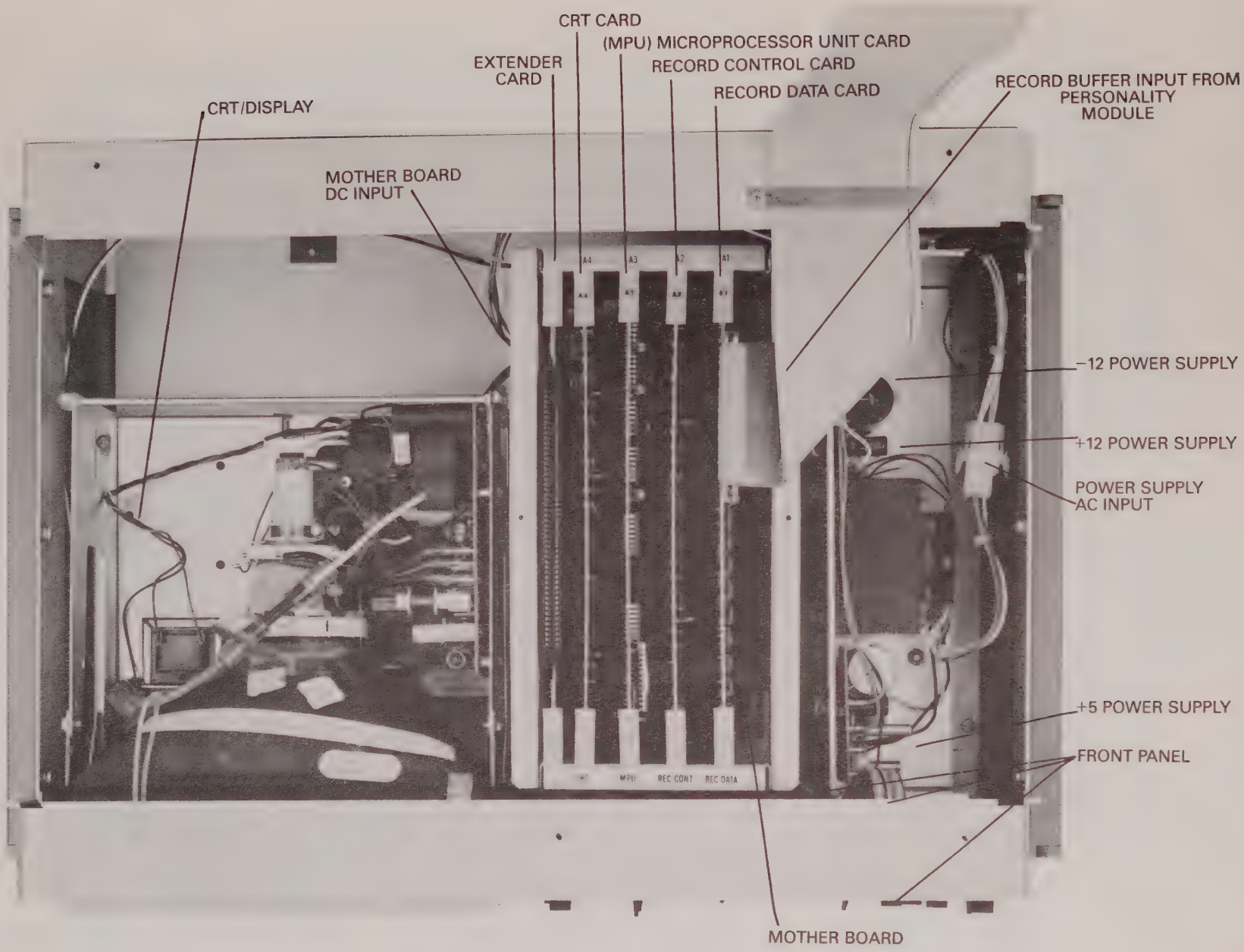



Figure 9.24 Internal Top View - PCB

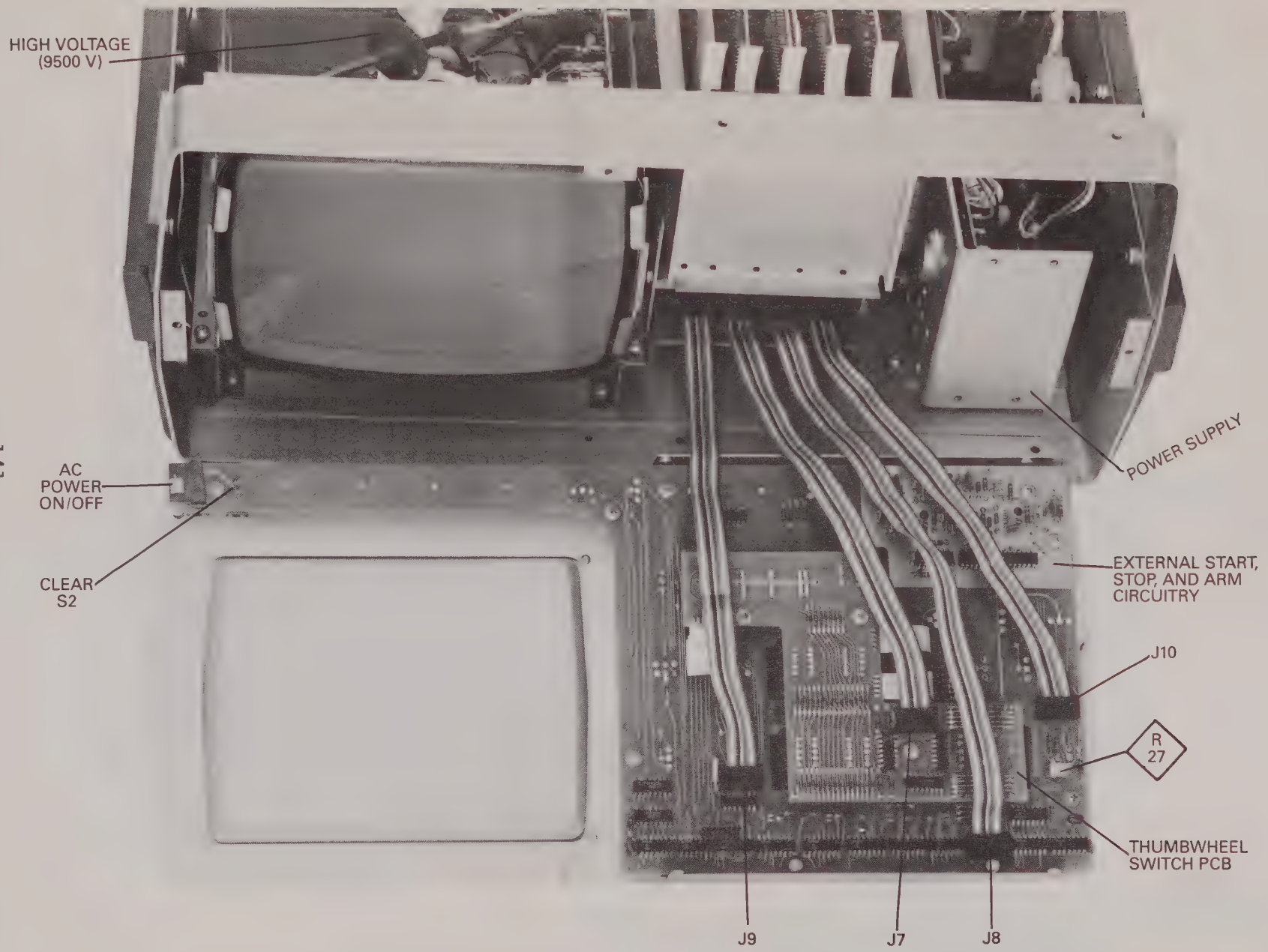



Figure 9.25 Internal Top View - Front Panel Disassembled

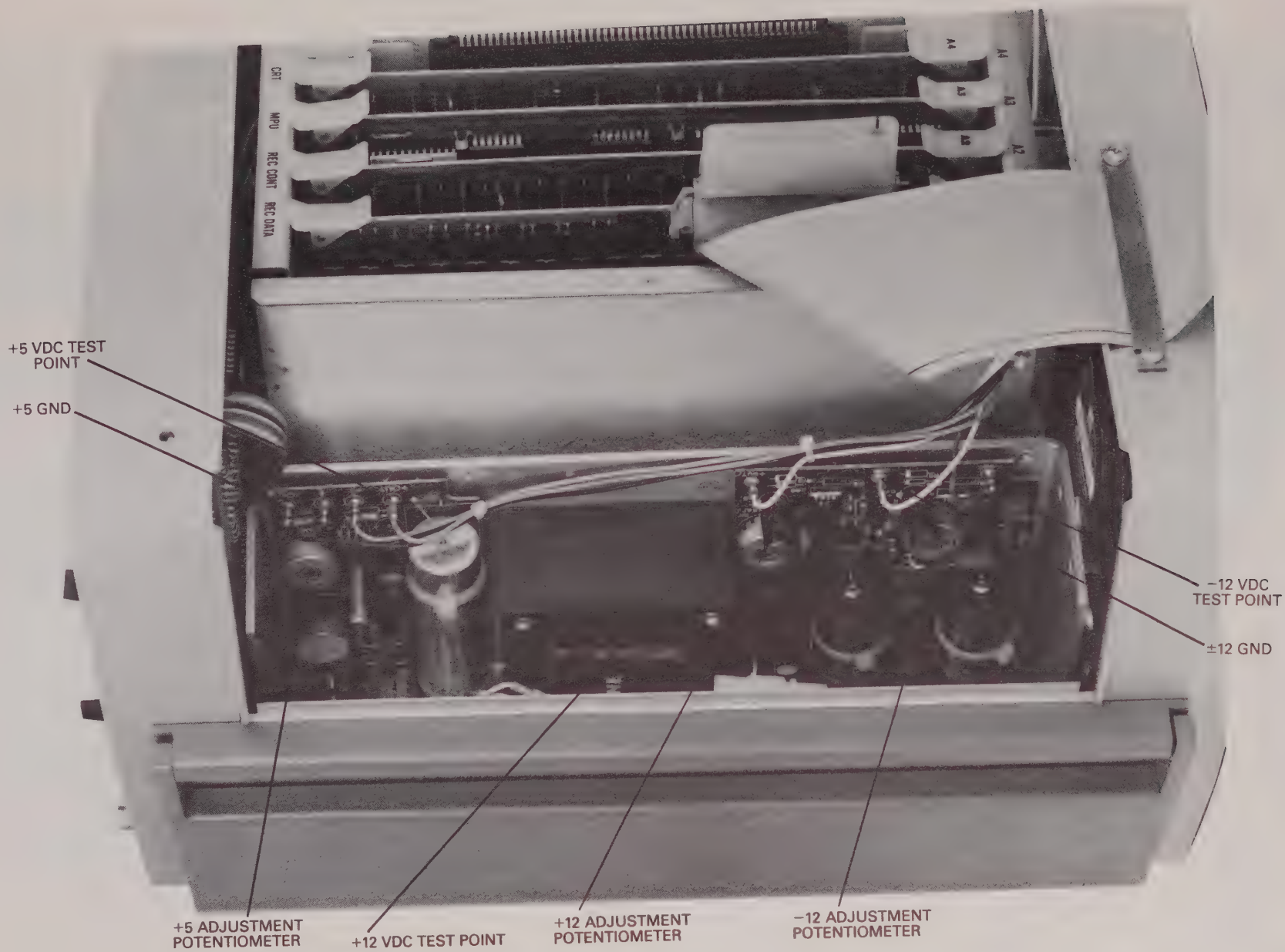



Figure 9.26 Internal Top View - Power

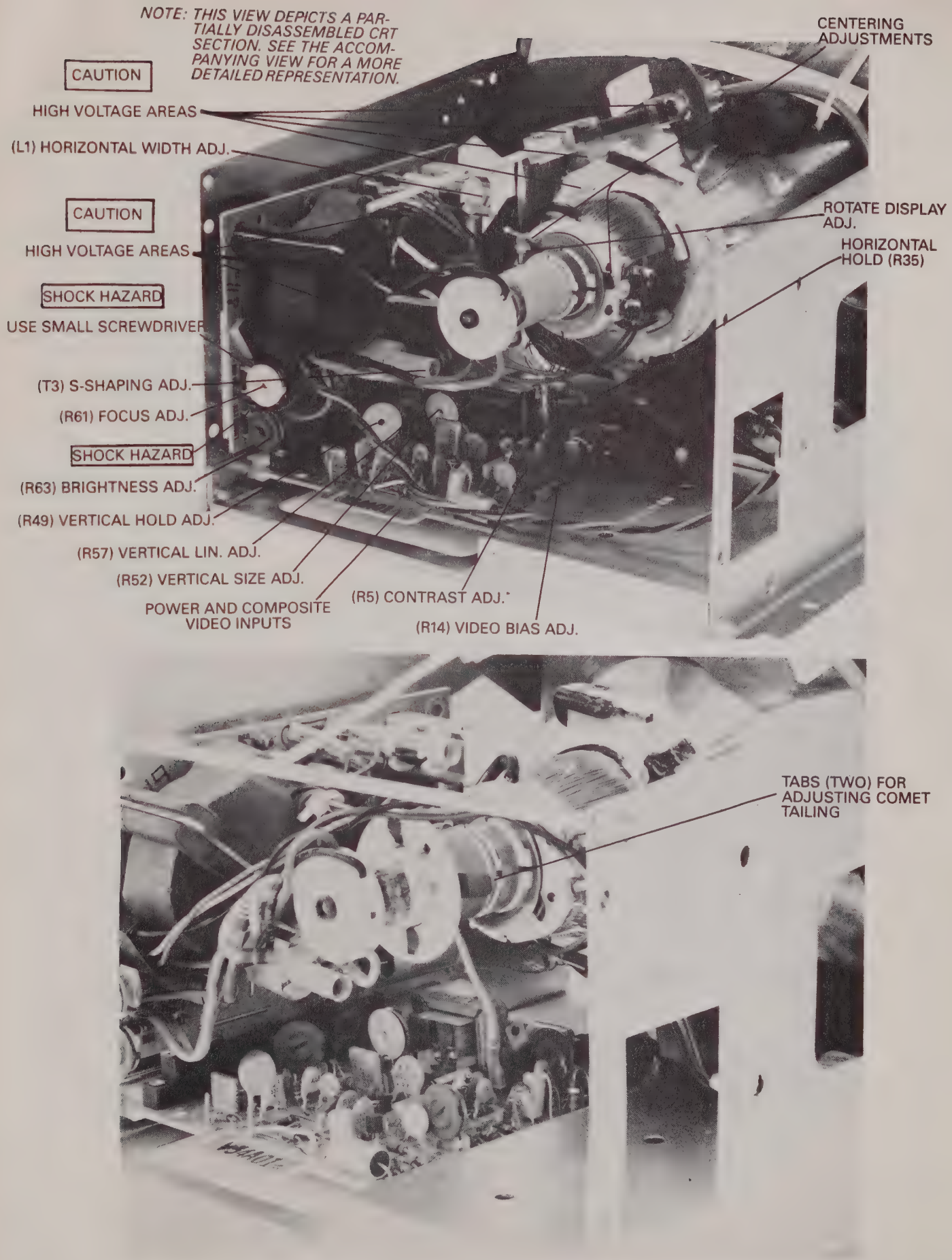
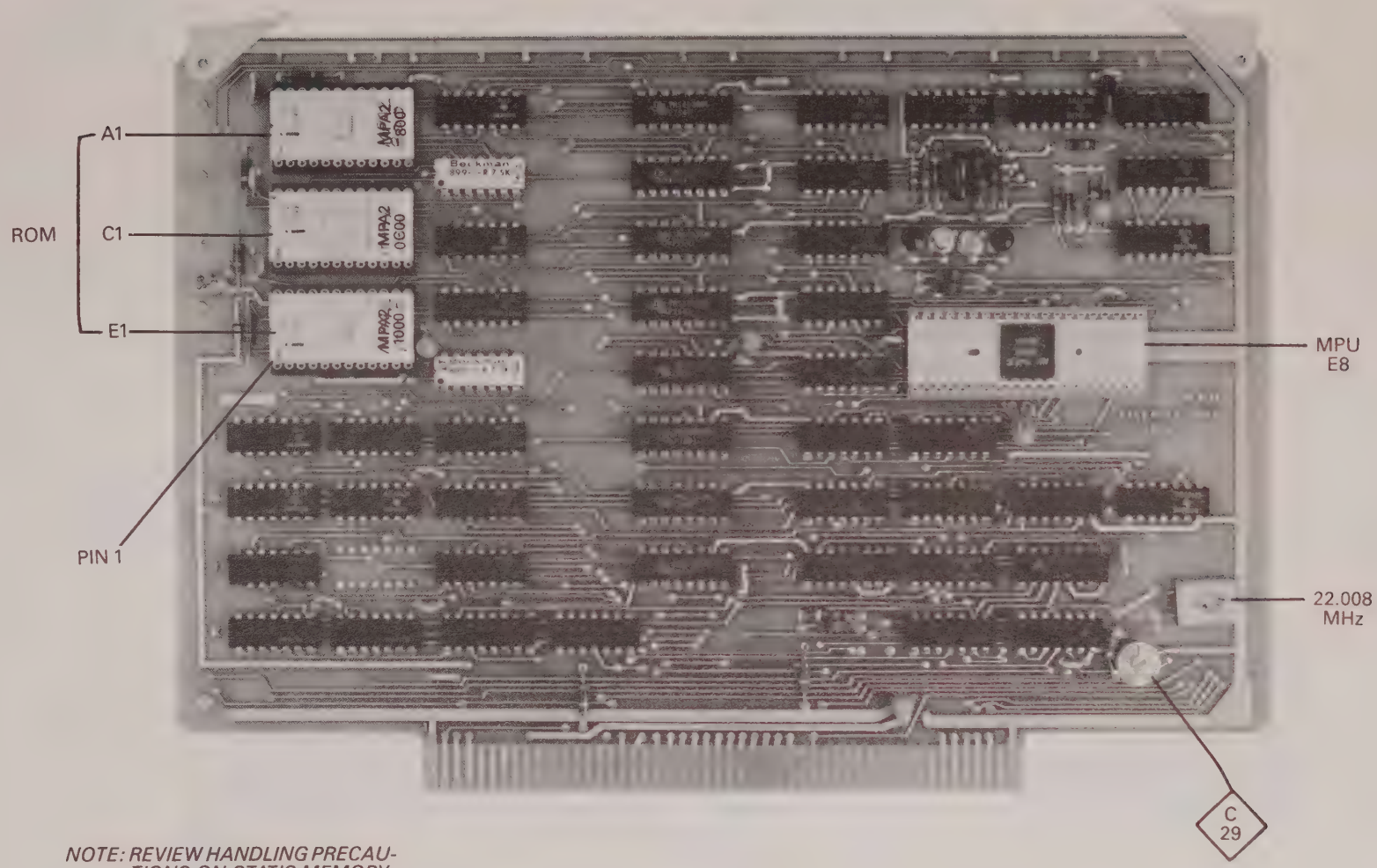



Figure 9.27 Rear View - CRT Section - Adjustments




*NOTE: REVIEW HANDLING PRECAUTIONS ON STATIC MEMORY DEVICES IN APPENDIX D PRIOR TO REMOVING THE ROM, RAM, OR MPU.*

Figure 9.28 MPU Card - Frequency Adjustments

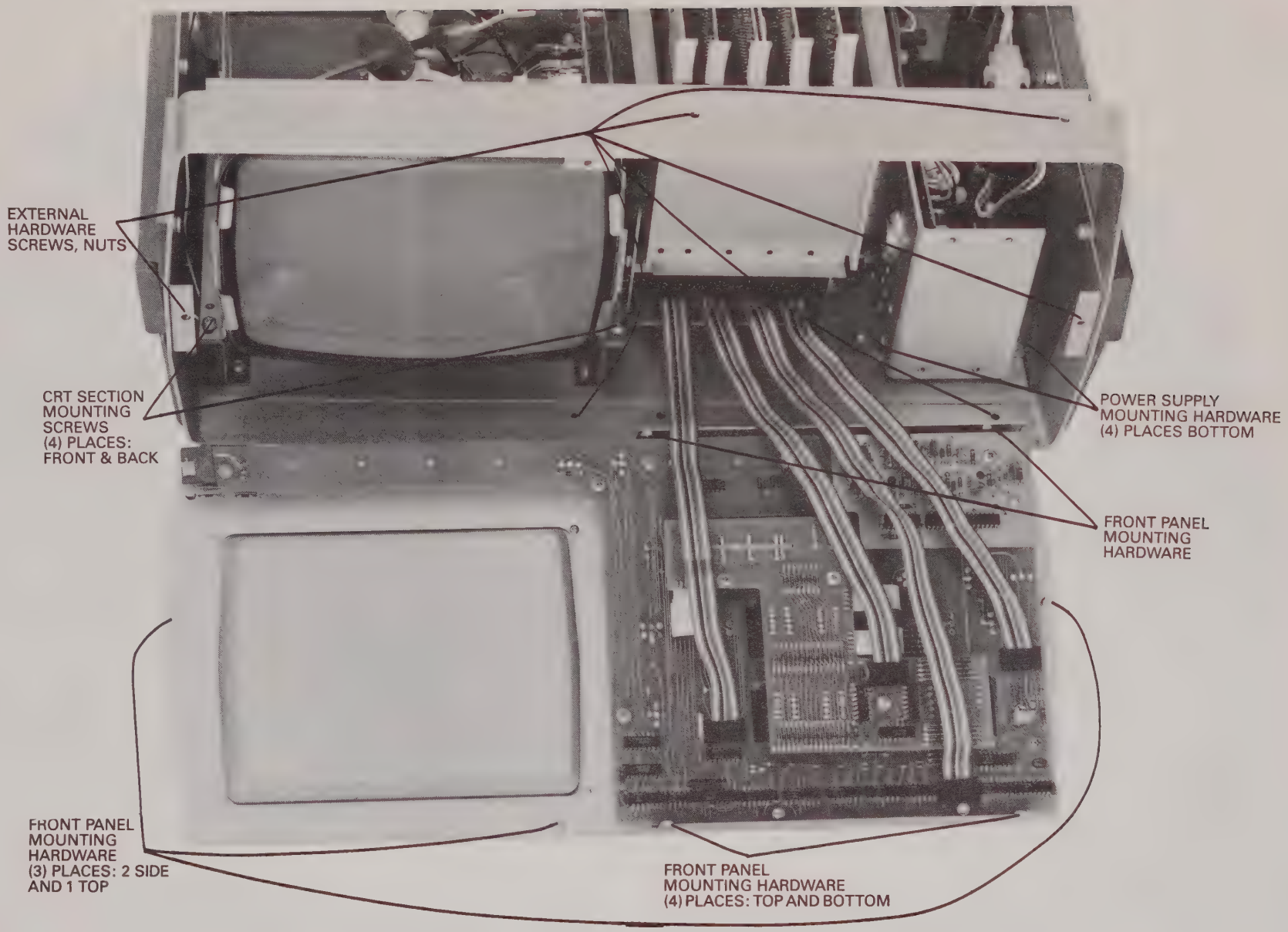
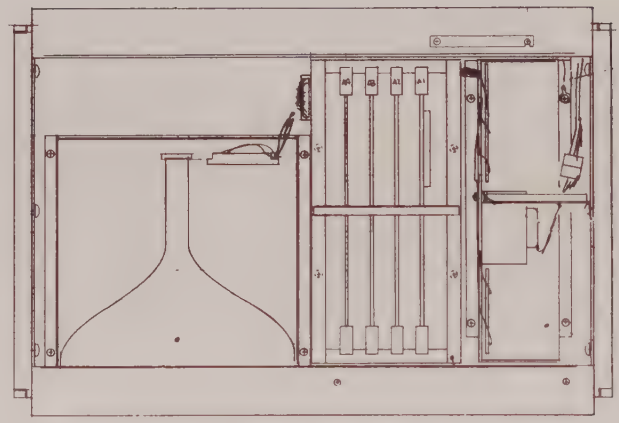



Figure 9.29 Internal Top View - Front Panel Hardware Locations



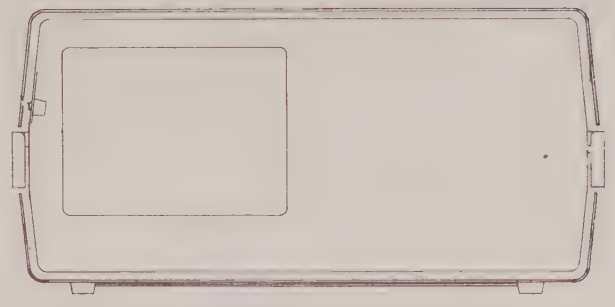



Figure 9.30 Top Assembly 168-D

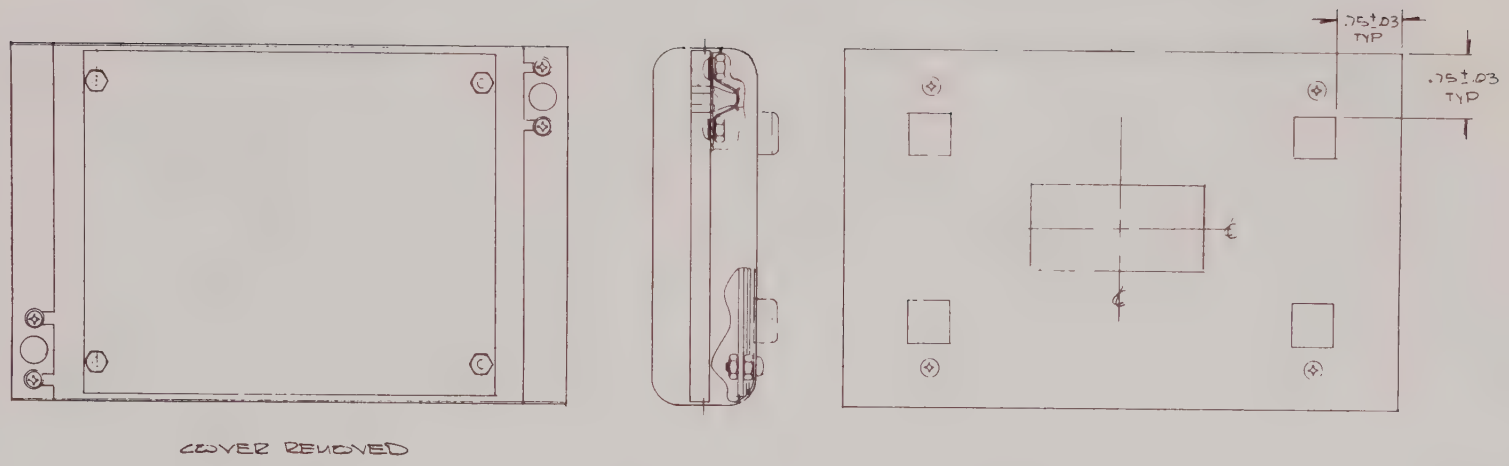



Figure 9.31 Personality Module Assembly

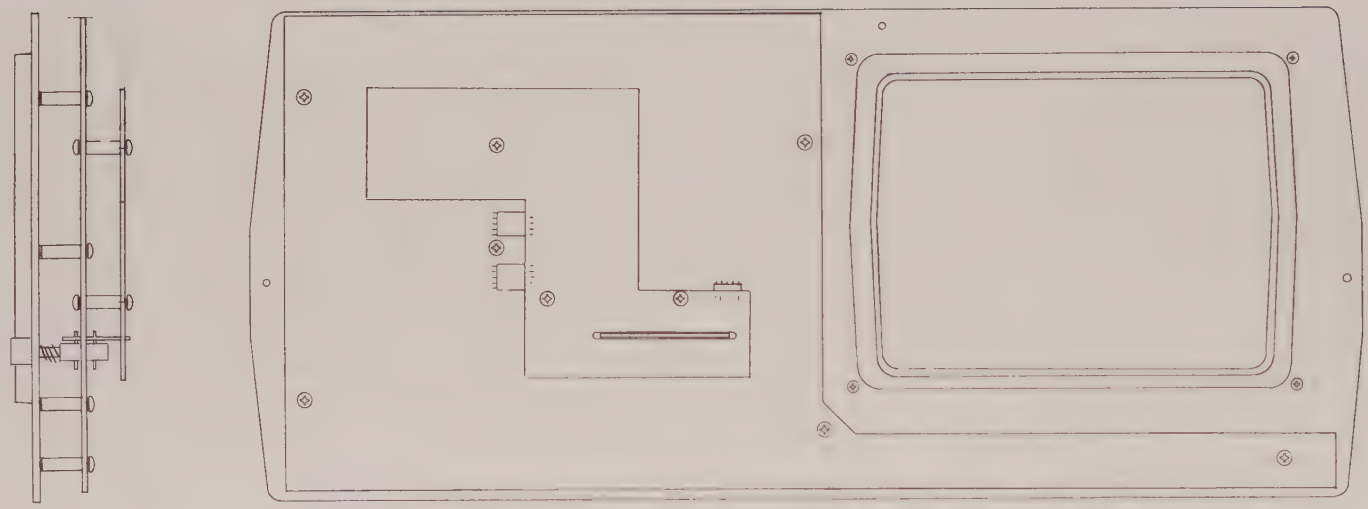


Figure 9.32 Front Panel Assembly

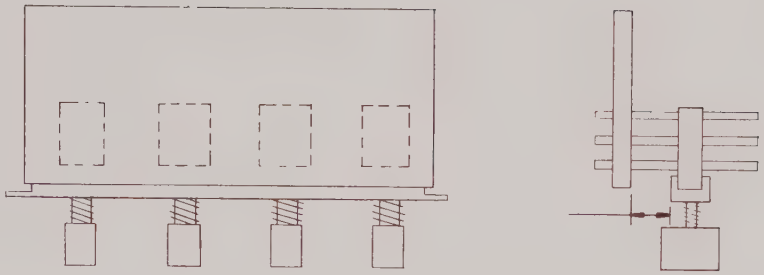


Figure 9.33 Display Select PCB Assembly

# APPENDICES

## SUPPLEMENTARY INFORMATION

### A.1 Introduction

The appendices in this section were included to supply additional information where needed.

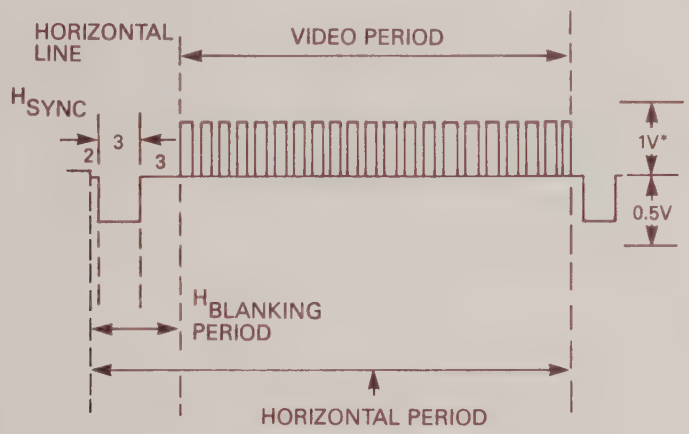
### A.2 List of Apendices


| | | Page |
|---|---|---|
| Appendix A | Character Display Formats | 151 |
| Appendix B | Motorola Service Manual (CRT) | 156 |
| Appendix C | Power-One Data Sheet (Power Supply) | 157 |
| Appendix D | Static Handling Precautions of MOS, LSI Logic | 159 |
| Appendix E | Mnemonics Table | 160 |

# APPENDIX A

## CHARACTER DISPLAY FORMATS

The following description assumes that the display will have high-speed scanning from left to right in the horizontal direction and low-speed scan from top to bottom in the vertical direction. Refer to Figure A-1.




*Video Amplitude: A 1.5 V pp video signal is typical and is preferred, but any signal from 0.5 V pp to 2.5 V pp with the same ratio as 1.5 V pp signal is usable.

Figure A-1. A Composite Video Signal

The term CHARACTER BLOCK is used to describe the total number of horizontal dots in a generated character plus the number of blank dots between characters. In the vertical direction, the term character block indicates the number of scan lines required to generate a character plus the blank scan lines between rows of characters.

CHARACTER RATE is the dot frequency divided by the actual dots per character. The dots per character determine the number of horizontal dots in a character block.

CHARACTER TIME is the reciprocal of the character rate.

The actual video period in a horizontal line is the total time of active character locations displayed on each row.

HORIZONTAL SYNC DELAY is the number of character time delays before horizontal sync. This interval is commonly called the "front porch." HORIZONTAL SYNC is the width of the horizontal sync pulse and should be defined in character times.

HORIZONTAL SCAN DELAY is the character times delay after horizontal sync prior to active scan. This interval is commonly called the horizontal sync "back porch."

The sum of the horizontal sync delay, horizontal sync, and horizontal scan delay is the HORIZONTAL BLANKING INTERVAL. This interval is required as a window in the horizontal scan period to allow retrace. The RETRACE time is internal to the CRT monitor; this time is a function of monitor horizontal scan components. This time, at a minimum, is the time it takes the display to return from the right to the left-hand side of the display. The retrace time is less than the horizontal blanking interval. Horizontal blanking time is normally about 20% of the total horizontal scanning period.

A practical system is to use a minimum of 25% of the characters per row for horizontal blanking (or approximately 20% of the character times per row). In an 80 character per row system this would give a total of 20 character times for the sum of the two delays plus sync. For systems operating at a horizontal scanning frequency of 15750 Hz (63.5 µsec period), RS170 compatible signals would be:

| Characters (Per Row) | H. Sync Delay | H. Sync | H. Scan Delay | Total Character Time/Row |
|---|---|---|---|---|
| 32 | 2 | 3 | 3 | 40 |

The preferable horizontal retrace time that would enable any system to be compatible with a wide variety of monitors would be in the range of 10.5 to 12 µsec, which is widely used in the industry.

HORIZONTAL PERIOD (For 15720 Hz horizontal frequency)

$$H_T = \frac{1}{15720} \text{ Hz} \quad 63.6 \text{ µsec}$$

HORIZONTAL BLANKING PERIOD (Refer to Figure A-2)

(Approximately 20% $H_T$)

$H_{BLANKING} = (0.20)\ (63.6\ \mu sec) = 12.7\ \mu sec$

VIDEO PERIOD (Refer to Figure A-3)

Horizontal Period - Horizontal Blanking Period)

$H_T - H_{BLANK} = 63.6\ \mu sec - 12.7\ \mu sec = 50.8\ \mu sec$

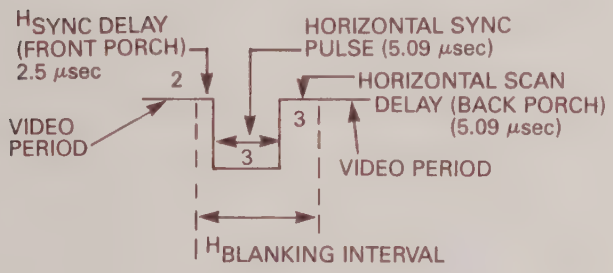



Figure A-2. An Approximate Timing of Horizontal Sync Within Blanking Period

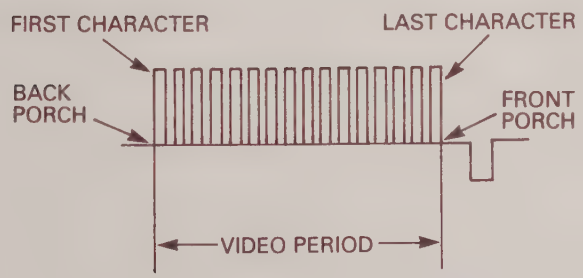



Figure A-3. Timing of Active Video Period Within Video Period

The required OSCILLATOR FREQUENCY is the desired horizontal scanning frequency times total character times per line times the number of dots per character block.

The VERTICAL SCANNING FREQUENCY can be obtained by the count down from the horizontal lines. The total number of scan lines generated for a vertical field equals the number of rows times the number of lines per character plus the vertical sync delay plus vertical sync plus the vertical scan delay.

LINES/CHARACTER is the number of horizontal lines in each character block.

ROWS are the number of displayed rows of characters.

VERTICAL SYNC DELAY is the number of scan lines delay before vertical sync.

VERTICAL SYNC is the width of the vertical sync pulse and should be expressed in scan line units.

VERTICAL SCAN DELAY is the delay between vertical sync and the next display information in scan line units.

Typical Settings: The sum of the vertical sync and the two delays is the vertical blanking interval. This interval is normally about 5% of the total number of scan lines. For the standard American TV system, the total scan lines in the noninterlaced mode is 262. The vertical scan rate (frame rate) is 60 Hz. Typical settings for evenly spaced noninterlaced patterns are as follows:

| Lines/CHR | Rows | V. Sync Delay | V. Sync | V. Scan Delay |
|---|---|---|---|---|
| 10 | 24 | 3 | 3 | 16 |

Refer to Figures A-4 and A-5.

VERTICAL PERIOD (for 60 Hz Vertical Refresh Rate)

$$V_T = \frac{1}{60\ Hz} = 16.67\ msec$$

VERTICAL BLANKING PERIOD (approximately 8% $V_T$)

$$V_{Blanking} = (0.08)\ \ (16.67\ msec) = 1.3\ msec$$

VIDEO PERIOD (Vertical Period - Vertical Blanking Period)

$$V_T - V_{BLANK} = 16.6\ msec - 1.3\ msec = 15.3\ msec$$

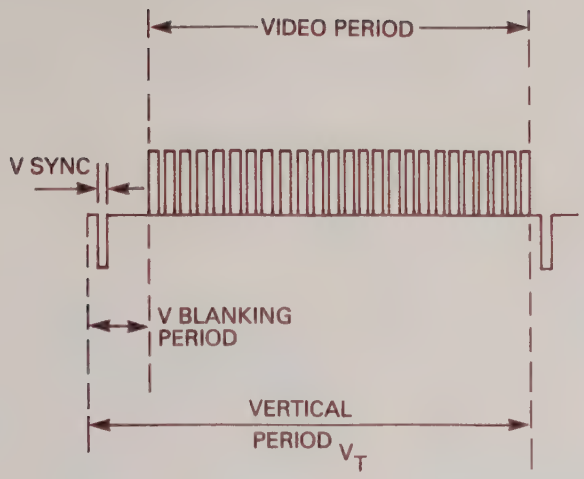



Figure A-4. Vertical Field

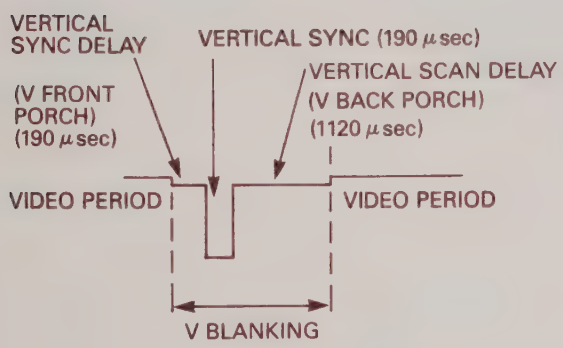



Figure A-5. Timing Vertical Sync Within Vertical Blanking Period

# MOTOROLA

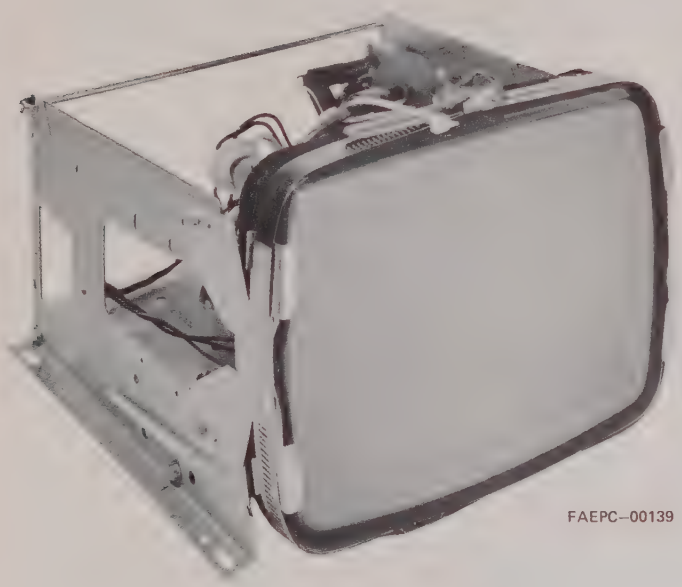
# Service Manual

# VP16

DATA PRODUCTS

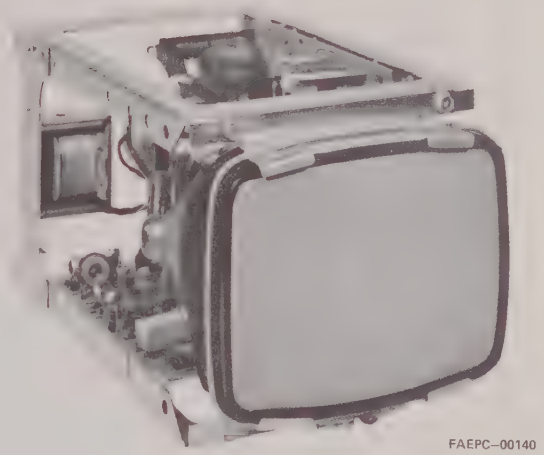
MODEL

**M1000-100**
**M1000-155**
**M2000-100**
**M2000-155**



FAEPC–00139

MODEL M2000 (9"–CRT)



FAEPC–00140

MODEL M1000 (5"–CRT)

## GENERAL INFORMATION

The models described herein are fully transistorized (except CRT) and applicable for displaying alphanumeric characters. The four models are as follows:

M1000–155 (5" CRT)/M2000–155 (9" CRT) – Operate with composite video inputs only.

M1000–100 (5" CRT)/M2000–100 (9" CRT) – Operate with separate TTL level vertical/horizontal sync and video inputs only.

The CRT'S employed are of the magnetic deflection type with integral implosion protection. An operating voltage of 12 volts DC @ 650 mA (typical) is required from an external power supply for the M1000 models. The M2000 models require an external 12 volts DC @ 900 mA (typical).

Input and output connections for the monitor are made through a 10–pin edge connector on the signal circuit card. Inputs consist of video, horizontal/vertical sync, +12 volts and ground. Output connections are provided for an optional remote brightness control.

Two plug–in etched circuit cards are utilized, a signal circuit card and a deflection circuit card. Components are mounted on the top of the circuit cards and copper foil on the bottom. Schematic reference numbers are printed on the top and bottom of each circuit card to aid in the location and identification of components for servicing. All standard operating/adjustment controls are mounted in a convenient manner on both circuit cards.

Circuitry consists of four stages for video amplification, six stages for horizontal/vertical sync and deflection processing, and one stage for video blanking during retrace. The M2000 models also provide dynamic focusing, which is a function of the horizontal output circuitry.

## CAUTION

NO WORK SHOULD BE ATTEMPTED ON ANY EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

**MOTOROLA Data Products** CAROL STREAM, ILLINOIS 60187

PART NO. 68P25253A23-1 3/77 PRICE $1.60
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PRINTED IN U.S.A.

# SAFETY WARNING

CAUTION: NO WORK SHOULD BE ATTEMPTED ON AN EXPOSED MONITOR CHASSIS BY ANYONE NOT FAMILIAR WITH SERVICING PROCEDURES AND PRECAUTIONS.

1. SAFETY PROCEDURES should be developed by habit so that when the technician is rushed with repair work, he automatically takes precautions.

2. A GOOD PRACTICE, when working on any unit, is to first ground the chassis and to use only one hand when testing circuitry. This will avoid the possibility of carelessly putting one hand on chassis or ground and the other on an electrical connection which could cause a severe electrical shock.

3. Extreme care should be used in HANDLING THE PICTURE TUBE as rough handling may cause it to implode due to atmospheric pressure (14.7 lbs. per sq. in.). Do not nick or scratch glass or subject it to any undue pressure in removal or installation. When handling, safety goggles and heavy gloves should be worn for protection. Discharge picture tube by shorting the anode connection to chassis ground (not cabinet or other mounting parts). When discharging, go from ground to anode or use a well insulated piece of wire. When servicing or repairing the monitor, if the cathode ray tube is replaced by a type of tube other than that specified under the Motorola Part Number as original equipment in this Service Manual, then avoid prolonged exposure at close range to unshielded areas of the cathode ray tube. Possible danger of personal injury from unnecessary exposure to X-ray radiation may result.

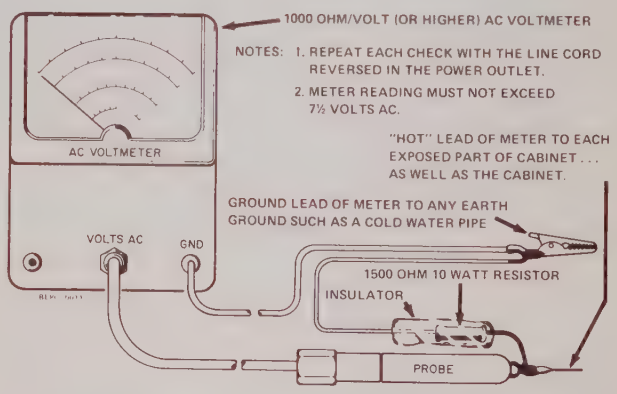
4. An ISOLATION TRANSFORMER should always be used during the servicing of a unit whose chassis is connected to one side of the power line. Use a transformer of adequate power rating as this protects the serviceman from accidents resulting in personal injury from electrical shocks. It will also protect the chassis and its components from being damaged by accidental shorts of the circuitry that may be inadvertently introduced during the service operation.

5. Always REPLACE PROTECTIVE DEVICES, such as fishpaper, isolation resistors and capacitors and shields after working on the unit.

6. If the HIGH VOLTAGE is adjustable, it should always be ADJUSTED to the level recommended by the manufacturer. If the voltage is increased above the normal setting, exposure to unnecessary X-ray radiation could result. High voltage can accurately be measured with a high voltage meter connected from the anode lead to chassis.

7. BEFORE RETURNING A SERVICED UNIT, the service technician must thoroughly test the unit to be certain that it is completely safe to operate without danger of electrical shock. DO NOT USE A LINE ISOLATION TRANSFORMER WHEN MAKING THIS TEST.

In addition to practicing the basic and fundamental electrical safety rules, the following test, which is related to the minimum safety requirements of the Underwriters Laboratories should be performed by the service technician before any unit which has been serviced is returned.


1000 OHM/VOLT (OR HIGHER) AC VOLTMETER
NOTES: 1. REPEAT EACH CHECK WITH THE LINE CORD REVERSED IN THE POWER OUTLET.
2. METER READING MUST NOT EXCEED 7½ VOLTS AC.
AC VOLTMETER
"HOT" LEAD OF METER TO EACH EXPOSED PART OF CABINET . . . AS WELL AS THE CABINET.
GROUND LEAD OF METER TO ANY EARTH GROUND SUCH AS A COLD WATER PIPE
VOLTS AC
GND
1500 OHM 10 WATT RESISTOR
INSULATOR
PROBE

Voltmeter Hook-up for Safety Check

A 1000 ohm per volt AC voltmeter is prepared by shunting it with a 1500 ohm, 10 watt resistor. The safety test is made by contacting one meter probe to any portion of the unit exposed to the operator such as the cabinet trim, hardware, controls, knobs, etc., while the other probe is held in contact with a good "earth" ground such as a cold water pipe.

The AC voltage indicated by the meter may not exceed 7½ volts. A reading exceeding 7½ volts indicates that a potentially dangerous leakage path exists between the exposed portion of the unit and "earth" ground. Such a unit represents a potentially serious shock hazard to the operator.

The above test should be repeated with the power plug reversed, when applicable.

NEVER RETURN A MONITOR which does not pass the safety test until the fault has been located and corrected.

**ELECTRICAL SPECIFICATIONS ***

| | MODEL M1000 | MODEL M2000 |
|---|---|---|
| PICTURE TUBE (CRT): | 5" measured diagonally (127 mm); 13 sq. in. viewing area (84 sq. cm); 55° deflection angle; P4 phosphor standard | 9" measured diagonally (228 mm); 44 sq. in. viewing area (284 sq. cm); 90° deflection angle; integral implosion protection; P4 phosphor standard |
| POWER INPUT: | 12V DC at 650 mA | 12V DC at 900 mA |
| INPUT SIGNALS: | COMPOSITE VIDEO INPUT; 0.5V to 2.5V composite P/P, sync negative (input impedance: 74 ohms terminated, 12k ohms unterminated), or<br>TTL SEPARATE HORIZONTAL, VERTICAL, VIDEO: 2.5V to 5.0V P/P, video drive, sync positive at input (input impedance: 75 ohms to 250 ohms video termination, >2k ohms vertical and horizontal) | |
| RESOLUTION: | 650 lines center, 500 lines corners | |
| VIDEO RESPONSE: | Within −3 dB,10 Hz to 12 MHz | |
| LINEARITY: | Within 2% as measured with standard EIA ball chart and dot pattern | |
| HIGH VOLTAGE: | 9.5 kV at 50 uA beam current, nominal | |
| HORIZONTAL RETRACE TIME: | 11.0 uSec maximum | |
| SCANNING FREQUENCY: | Horizontal: 15,750 Hz ±500 Hz; Vertical: 50/60 Hz | |
| ENVIRONMENT: | Operating temperature: 0° C to 50° C<br>Storage temperature: −40° C to +65° C<br>Operating altitude: 10,000 feet maximum (3048 meters)<br>Designed to comply with applicable DHEW rules on X-Radiation<br>Designed to enable listing under UL Specification 478 | |
| TYPICAL DIMENSIONS: | 4.60" H, 5.12" W, 8.68" D (without power supply) (117 x 130 x 220 mm) | 7.25" H, 9.50" W, 9.48" D (184 x 241 x 241 mm) |

* Specifications subject to change without notice.

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## SERVICE NOTES

### CIRCUIT TRACING

Component reference numbers are printed on the top and bottom of the plug–in circuit cards to facilitate circuit tracing. In addition, control names and circuit card terminal numbers are also shown and referenced on the schematic diagrams in this manual.

Transistor elements are identified as follows:

E – emitter, B – base, and C – collector.

### COMPONENT REMOVAL

Removing components from an etched circuit card is facilitated by the fact that the circuitry (copper foil) appears on one side of the circuit card only and the component leads are inserted straight through the holes and are not bent or crimped.

It is recommended that a solder extracting gun be used to aid in component removal. An iron with a temperature controlled heating element would be desirable since it would reduce the possibility of damaging the circuit card foil due to over–heating.

The nozzle of the solder extracting gun is inserted directly over the component lead and when sufficiently heated, the solder is drawn away leaving the lead free from the copper foil. This method is particularly suitable in removing multi-terminal components.

### POWER TRANSISTOR REPLACEMENT

When replacing the "plug–in" transistor, please observe the following precautions:

1. The transistor heat sink is not "captive", which means that the transistor mounting screws also secure the heat sink. When installing the transistor, the heat sink must be held in its proper location.

2. When replacing the plug–in transistor, silicone grease (Motorola Part No. 11M490487) should be applied evenly to the top of the heat sink and bottom of the transistor.

3. The transistor mounting nuts must be tight before applying power to the monitor. This insures proper cooling and electrical connections. NON–COMPLIANCE WITH THESE INSTRUCTIONS CAN RESULT IN FAILURE OF THE TRANSISTOR AND/OR ITS RELATED COMPONENTS.

**— NOTE —**

Use caution when tightening transistor mounting nuts. If the screw threads are stripped by excessive pressure, a poor electrical and mechanical connection will result.

### CRT REPLACEMENT

Use extreme care in handling the CRT as rough handling may cause it to implode due to high vacuum. Do not nick or scratch glass or subject it to any undue pressure in removal or installation. Use goggles and heavy gloves for protection. In addition, be sure to disconnect the monitor from all external voltage sources.

1. Discharge CRT by shorting 2nd anode to ground; then remove the CRT socket, deflection yoke and 2nd anode lead.

2. Remove CRT from chassis by loosening the one screw that secures the CRT mounting strap or retaining ring.

### HORIZONTAL OSCILLATOR ADJUSTMENT

Step 1. Turn on monitor and set up for normal operation.

Step 2. Locate the HORIZ. HOLD control, R35, on the Signal circuit card.

Step 3. Begin rotating R35 CCW until the video display is out of horizontal sync. At this point rotate R35 back CW until the video display just locks in horizontally; then stop. Using tape, mark the left–hand edge of the video display (not the raster edge) of the CRT faceplate.

Step 4. Continue rotating R35 CW until the video display is out of horizontal sync again in the opposite direction. At this point rotate R35 back CCW until the video just locks in horizontally; then stop. Mark the left–hand edge of the video display on the CRT faceplate again.

Step 5. Observe the distance between the two marks on the CRT faceplate. The object is to rotate the HORIZ. HOLD control, R35, until the left–hand edge of the video display is centered between the two marks on the CRT faceplate.

### VIDEO BIAS ADJUSTMENT

Step 1. With the monitor operating, rotate the CONTRAST control, R6, for minimum contrast; then disconnect the input signal(s).

Step 2. Connect a voltmeter across R18 (negative probe toward the collector of Q4).

Step 3. Adjust the VIDEO BIAS control, R14, for a +1.0 ±.05 volt indication.

Step 4. Disconnect the voltmeter.

Step 5. Reconnect the input signal(s) and adjust the CONTRAST control, R6, for desired contrast.

### HORIZONTAL LINEARITY ADJUSTMENT

**— NOTE —**

This adjustment procedure is required only when a CRT and/or deflection yoke have been replaced.

PROCEDURE

Step 1. Disconnect monitor from power supply.

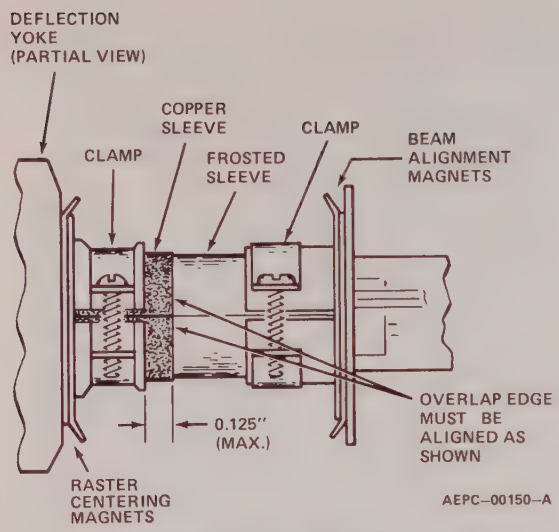



**Figure 1. Partial View of CRT Neck/Deflection Yoke for Horiz. Linearity Adjustment**

Step 2. (M2000 ONLY) Locate the S–SHAPING transformer, T3, on the deflection circuit card; then rotate its slug down to the bottom. (This action temporarily minimizes the effect of T3 being in the circuit.)

Step 3. (Refer to Figure 1.) Loosen the deflection yoke clamp screw just enough to permit sliding the copper sleeve on the CRT neck back and forth.

Step 4. (Refer to Figure 1.) Position the copper sleeve so that only 1/8" (.125") extends out past the rear lip of the deflection yoke. In addition, be sure that the overlap edge of the copper sleeve is aligned properly and not twisted.

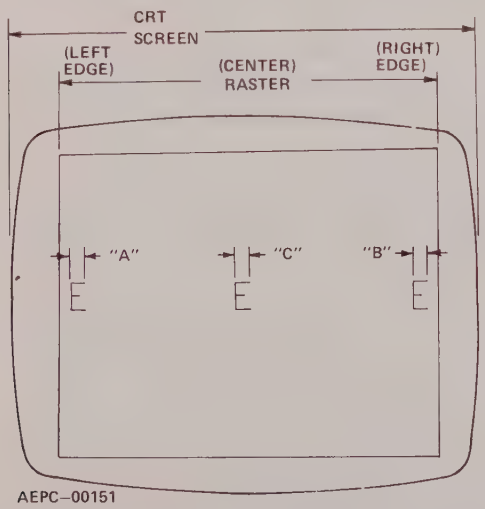



**Figure 2. Partial CRT Raster Display of Characters for Adjustment**

Step 5. Tighten the clamp screw carefully so as not to disturb the yoke position.

Step 6. Connect the monitor to its power supply and set up for normal operation.

Step 7. (Refer to Figure 2.) Observe the extreme left-hand edge characters (designated "A" in Figure 2). Its width should be equal to the width of the right–hand edge characters (designated "B" in Figure 2). If character "A" is wider than character "B", the copper sleeve is extending out too far. If "A" is narrower than "B", the copper sleeve should be pulled out further. In any event, the copper sleeve may have to be repositioned by trial and error if the 0.125–inch dimension does not provide desired linearity. Continue until the width of character "A" is equal to the width of character "B".

— NOTE —

Steps 8–11 are applicable only for the M2000 monitor.

Step 8. With the M2000 monitor turned on and operating normally, observe the width of the center character (designated "C" in Figure 2). It should be narrower than characters "A" and "B".

Step 9. Connect an oscilloscope (AC coupled) between the blue wire pin (on deflection circuit card) and chassis ground. A parabolic waveform should appear.

Step 10. Begin rotating the slug of T3 upward (away from circuit card) until the amplitude of the waveform is 125 volts P–P. This setting will equalize the width of character "C" to that of characters "A" and "B".

Step 11. Disconnect oscilloscope.

## RASTER CENTERING (Figure 1)

Step 1. Position the tabs of the beam alignment magnets such that they are horizontally opposing.

Step 2. Adjust vert. size (R52) and horiz. width (L1) such that all edges of the raster are visible.

Step 3. Position centering magnets for best centering of display raster.

## CRT BEAM ALIGNMENT

For optimum character quality in the corners of the video display, a beam alignment magnet may be used on the monitor CRT.

— NOTE —

Adjustment of the raster centering rings must precede the adjustment of the beam alignment rings.

### PROCEDURE

The beam alignment magnet should be positioned on the neck of the CRT between the deflection yoke and the tube base. The correct location of the rings is approximately over the second grid of the election gun (Figure 1).

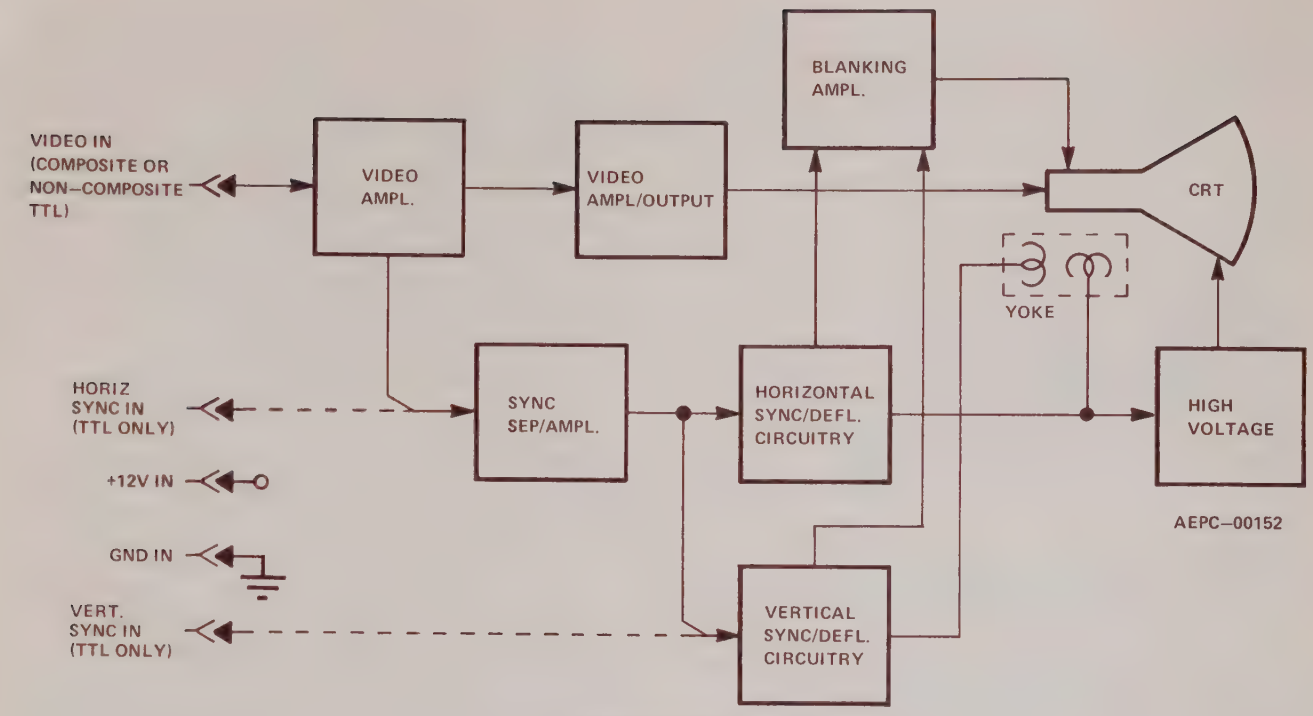
Step 1. Adjust the display brightness for optimum viewing.

Step 2. Adjust the focus voltage for optimum overall focus.

Step 3. Loosen the clamping screw just enough to allow the assembly free movement on the CRT neck.

Step 4. While observing the tails on the dots in the corners of the display, rotate the focus rings to minimize the tails.

Step 5. Tighten the clamping screw.




**Block Diagram**

## THEORY OF OPERATION

### GENERAL

The following circuit description is applicable to monitors using a composite video signal as its input. For monitors using TTL inputs, the description is basically the same. However, the horizontal and vertical sync pulses are coupled from an external source through separate inputs, as is the non–composite video. In addition, jumpers JU1 and JU2 will be inserted in the TTL position.

### VIDEO AMPLIFIER CIRCUIT

(Reference Figure 3.)

The video amplifier consists of four stages that include Q1, Q2, Q3 and Q4. The first stage, Q1, functions as an emitter follower. The low output impedance of this first stage permits use of a low resistance CONTRAST control, R6, which furnishes flat video response over its entire range without the need for compensation. The collector output of Q1 is used to drive the sync separator, Q5. Capacitor C2 provides high frequency roll–off to limit the collector output to the bandwidth required to pass synchronization signals.

Transistors Q2 and Q3 form a direct coupled amplifier with frequency compensation provided by C40 and C41. The output from Q3 is capacitively coupled (C5) to the base of Q4, video output stage. The video bias control, R14, is used to set the quiescent collector current of Q4. Frequency compensation is provided by R17 and C6. The combined action of clamping diode D1 and capacitor C5 provide DC restoration for the video signal.

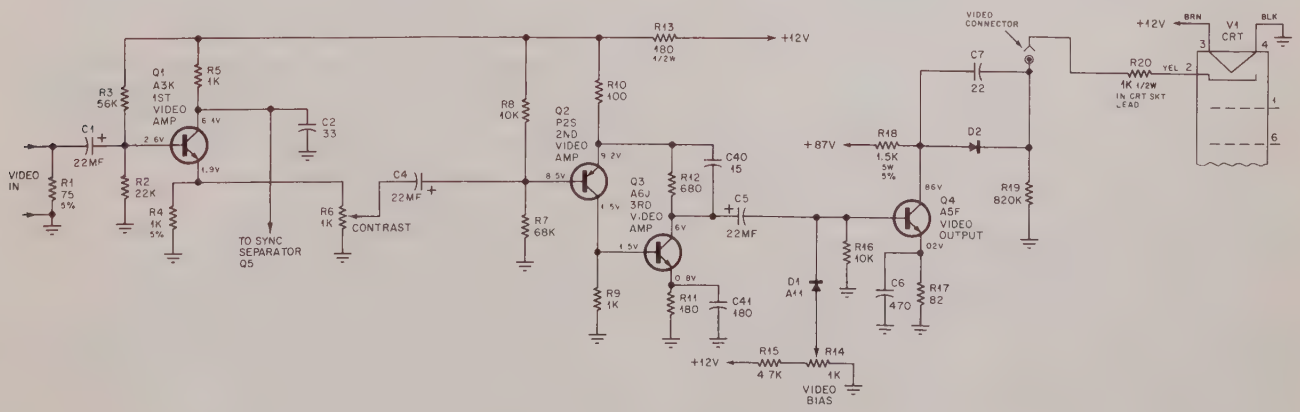



**Figure 3. Video Amplifier Circuit**

Components C7, D2 and R19 provide CRT beam current limiting. Diode D2 is normally forward–biased; therefore, as Q4 conducts, its collector voltage drops. This causes a larger beam current to flow through R19, which in turn causes its voltage drop to rise. If excessive beam current flows, the voltage developed across R19 becomes greater than the collector voltage of Q4. This action reverse-biases D2, which prevents a further increase in beam current. Capacitor C7 helps couple video to the CRT cathode, pin 2, through R20. Resistor R20 is used to isolate Q4 from transients that may occur as a result of CRT arcing.

## SYNC SEPARATOR/AMPLIFIER CIRCUIT

(Reference Figure 4.)

The sync separator employs two stages. Transistor Q5 is the sync separator and Q6 is the sync amplifier. The video input to the sync separator is black positive. Capacitor C3 is charged by the peak base current that flows when the positive peak of the input takes Q5 to saturation. This charge depends on the peak to peak input to Q5 and thus makes the bias for Q5 track the amplitude of the input signal. As a result, Q5 amplifies only the positive peaks of the input signal. The initial bias current through R23 sets the clipping level.

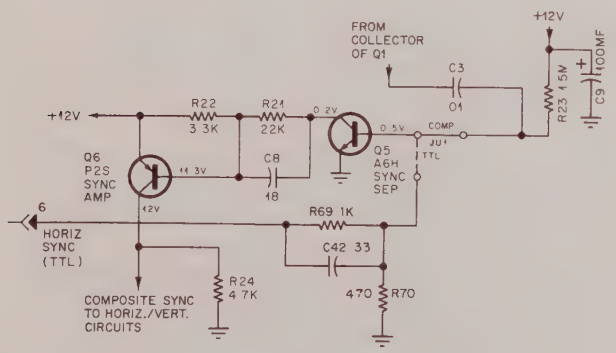



**Figure 4. Sync Separator/Amplifier Circuit**

## PHASE DETECTOR (AFC)

(Reference Figure 5.)

The phase detector control consists of two diodes (D3 & D13) in a keyed clamp circuit. Two inputs are required to generate the required output, one from the sync amplifier, Q6, and one from the horizontal output circuit, Q8. The required output must be of the proper polarity and amplitude to correct phase differences between the input horizontal sync pulses and the horizontal time base. The horizontal output (Q8) collector pulse is integrated into a sawtooth by R28, C13 and R29. During horizontal sync time, both diodes conduct, which shorts C13 to ground. This effectively clamps the sawtooth on C13 to ground at sync time. If the horizontal time base is in phase with the sync (waveform A), the sync pulse will occur when the sawtooth is passing through its AC axis and the net charge on C13 will be zero (waveform B). If the horizontal time base is lagging the sync, the sawtooth on C13 will be clamped to ground at a point negative from the AC axis. This will result in a positive DC charge on C13 (waveform C). This is the correct polarity to cause the horizontal oscillator to speed up to correct the phase lag. Likewise, if the horizontal time base is leading the sync, the sawtooth on C13 will be clamped at a point positive from its AC axis. This results in a net negative charge on C13, which is the required polarity to slow the horizontal oscillator (waveform D).

Passive components R30, R31 and C16 comprise the phase detector filter. The bandpass of this filter is chosen to provide correction of horizontal oscillator phase without ringing or hunting. Optional capacitor C14 (when present) times the phase detector for correct centering of the picture on the raster.

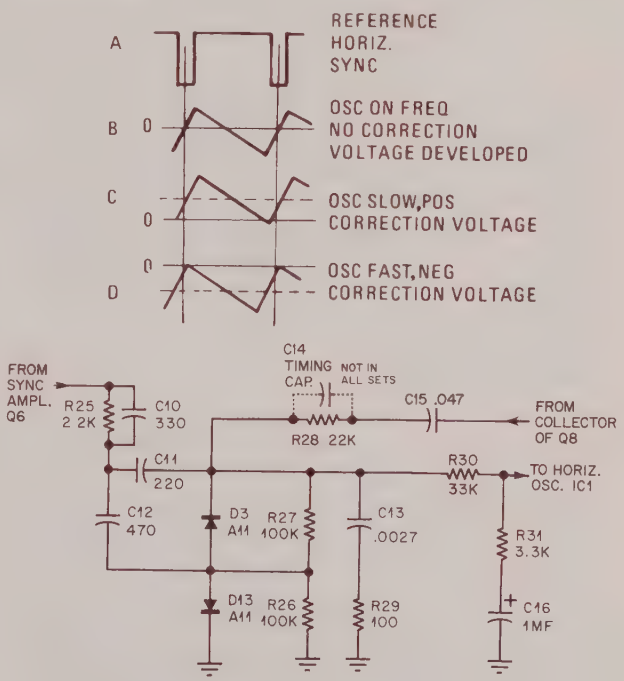



**Figure 5. Phase Detector (AFC) Circuit**

## HORIZONTAL OSCILLATOR AND DRIVER

(Reference Figure 6.)

The horizontal oscillator consists of integrated circuit IC1, which is essentially a voltage controlled oscillator with variable mark–space ratio (duty cycle) and internal voltage reference. The reference voltage is present at pin 6, while resistors R37 and R38 determine the mark–space ratio. The main oscillator timing capacitor is C17, with its charging current derived from three sources: (a) a fixed current from R33, (b) a variable current from R34 and HORIZ. HOLD control R35, (c) and a correcting current from the phase detector (AFC) network through R32. The combination of these three charging currents and C17 determine the horizontal frequency.

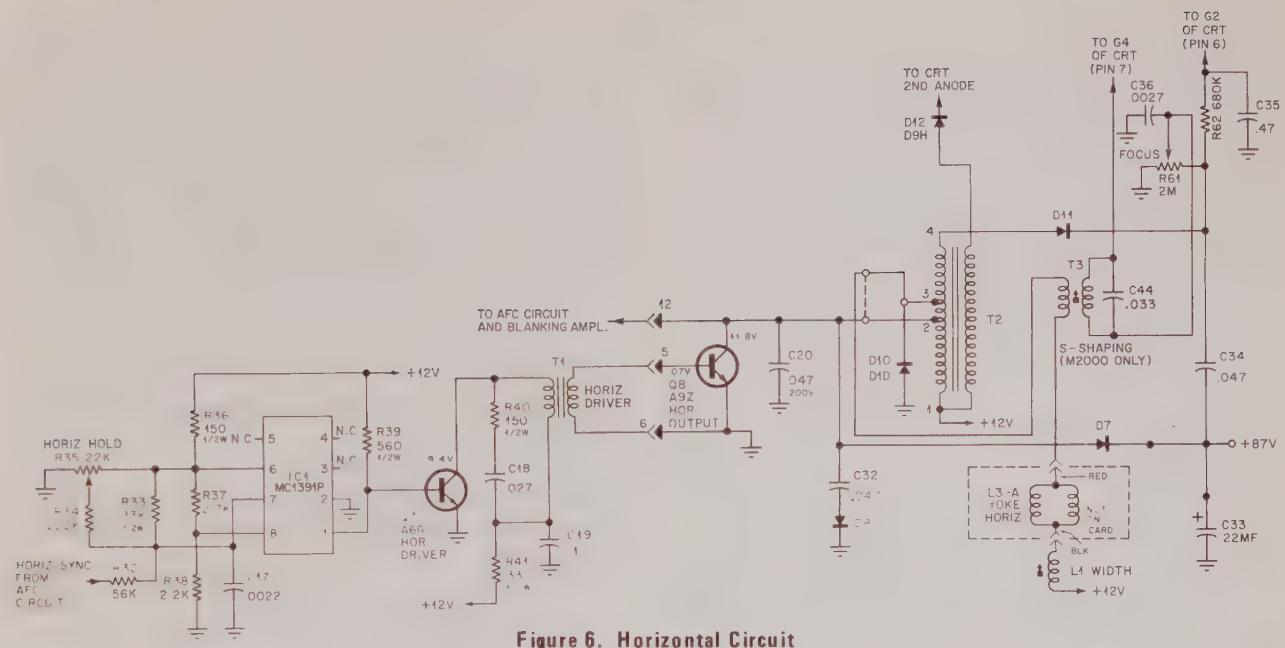



**Figure 6. Horizontal Circuit**

The output from IC1 (pin 1) is a square wave of proper frequency and duration, which is applied to the base of horizontal driver Q7. The output from Q7 is coupled via the horizontal driver transformer T1 (current step–up) to the base of horizontal output device Q8. Components R41 and C19 provide current limiting, while components R40 and C18 provide transformer damping to suppress ringing in the primary of T2 when Q7 goes into cutoff.

## HORIZONTAL OUTPUT

(Reference Figure 6.)

The secondary of T1 provides the required low drive impedance for Q8. Once during each horizontal period, Q8 operates as a switch that connects the supply voltage across the parallel combination of the horizontal deflection yoke (L3–A) and the primary of the high voltage transformer, T2. The required sawtooth deflection current (through the horizontal yoke) is formed by the L–R time constant of the yoke and primary winding of transformer T2. The horizontal retrace pulse charges C33 through D7 to provide +87V.

Momentary transients at the collector of Q8, should they occur, are limited to the voltage on C33 since D7 will conduct if the collector voltage exceeds this value.

The damper diode, D10, conducts during the period between retrace and turn on of Q8. Capacitor C20 is the retrace tuning capacitor. Coil L1 is a series HORIZ. WIDTH control. Components C32 and D8 generate a negative voltage necessary to properly bias the CRT. A copper sleeve on the neck of the CRT shapes the horizontal magnetic field for proper linearity.

Pin 4 of the high voltage transformer, T2, is a boost winding, which together with components D11 and C34, develops a +400 volts for G2 of the CRT. This same +400 volts is also always present on the high side of FOCUS control R61.

— NOTE —

In the M2000 monitor (only), an S–shaping transformer, T3, and capacitor C44 provide additional shaping of the horizontal deflection yoke current for proper linearity.

## VERTICAL OSCILLATOR, DRIVER AND OUTPUT

(Reference Figure 7.)

Composite sync pulses from the collector of Q6, Sync Ampl., are applied to the double integrating network of R45, C23, R46 and C24. The horizontal component of the sync signal is removed, leaving only the vertical sync pulses. The vertical sync pulses are coupled to the free running vertical oscillator stage, Q10, by C25 and R47. Transistors Q10 and Q12 are connected as a multivibrator. Transistor Q11 is used as an emitter follower that provides a low impedance drive for the vertical output stage, Q12. The series combination of capacitors C27 and C28 are initially charged to the supply voltage through R53 and the VERT. SIZE control, R52, which generates an exponential ramp of voltage.

When a positive vertical sync pulse is applied to the base of Q10, it begins conducting, which immediately discharges C27 and C28. This action turns off Q11 and causes a sudden decrease in the collector current of Q12, which also decreases the vertical deflection current through deflection yoke (L3–B) and vertical choke (L2). The resultant rapidly collapsing field in L2 generates a large voltage spike that is used for vertical retrace. Components R58, C29, R51 and C26 shape this spike to ensure that Q10 remains conducting until retrace is carried out to completion. Diode D4 couples the shaped spike to the base of Q10. At this point, Q10 reverts to its non–conducting state and the cycle repeats. The VERT HOLD control, R49, and R48,

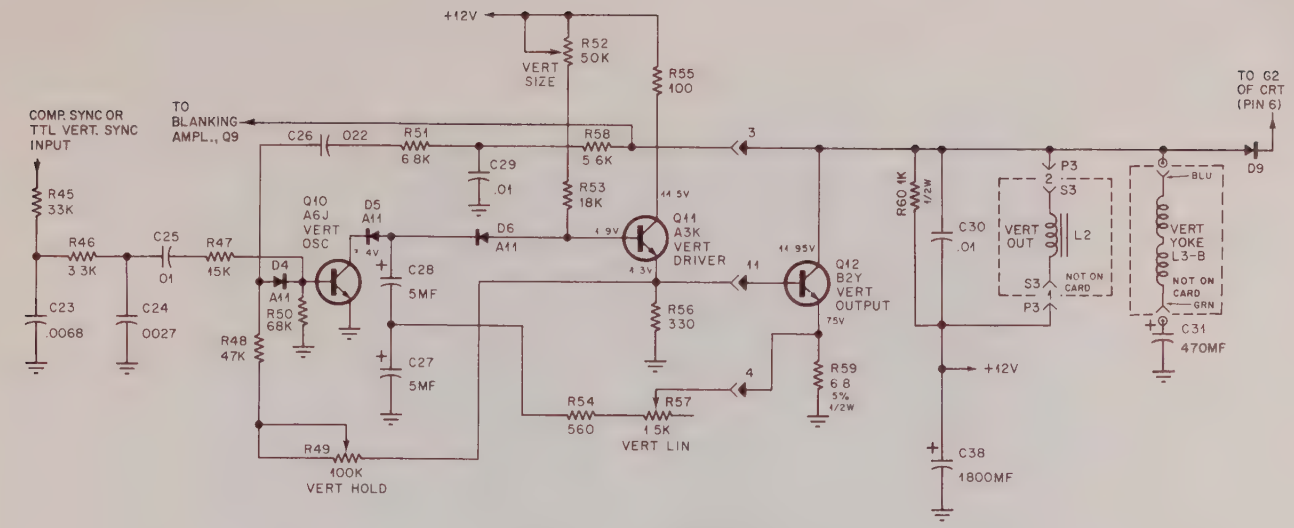
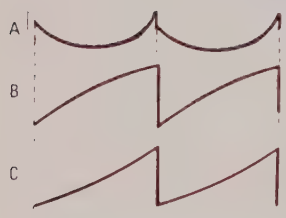



**Figure 7. Vertical Circuit**




PARABOLA AT JUNCTION OF C27 AND C28

VERTICAL DRIVE WITHOUT VERT PARABOLA ADDED

PARABOLA PULSE AND VERTICAL SAWTOOTH ADDED TOGETHER, WHICH PRODUCES THE REQUIRED VERT DRIVING SIGNAL.

provide a feedback signal to Q10 to maintain oscillation in the event vertical sycn pulses are not present. Diodes D5 and D6 provide the proper voltage drops to operate Q12 class A.

Vertical linearity is maintained by applying the ramp voltage generated across R59, through R57 (VERT LIN control) and R54, to the junction of C27 and C28. Since this path is resistive, the waveform will be integrated into a parabola by C27 (waveform A). This results in a predistortion of the ramp waveform (waveform C). (Waveform B illustrates the drive sawtooth without parabola shaping.) Parabolic shaping is necessary to compensate for the nonlinear charging of C27 and C28, and the impedance change occuring in L2 with current. Capacitor C31 serves to remove the DC component of the vertical deflection yoke current. Diode D9 clamps the collector voltage of Q12 to a safe level.

## RETRACE BLANKING

(Reference Figure 8.)

Retrace blanking is provided by negative–going horizontal and vertical rate pulses applied to G1 of the CRT. The collector pulse from the horizontal output stage, Q8, is developed across R43 through R42 and C22. The collector pulse from the vertical output stage, Q12, is differentiated by C21 to remove the sawtooth portion of the waveform. The remaining pulse appears across R43. The mixed vertical and horizontal pulses on R43 are amplified and inverted by the blanking amplifier, Q9, and applied to G1 of the CRT.

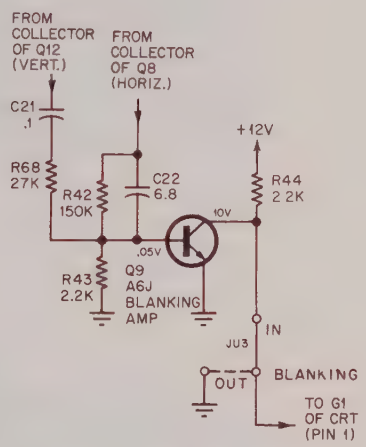


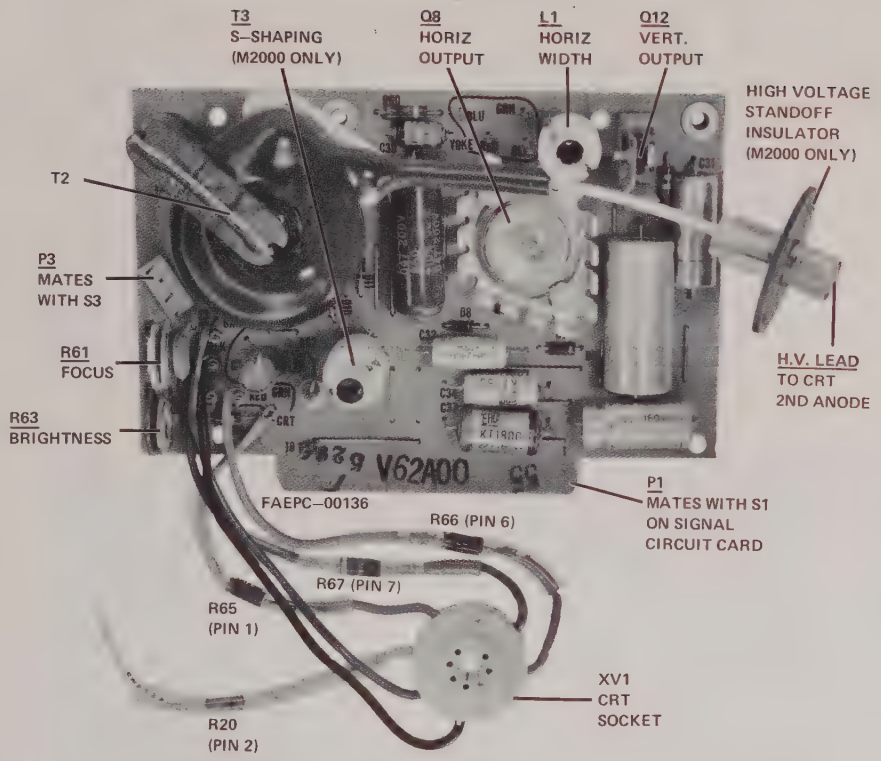

**Figure 8. Blanking Amplifier**

## DYNAMIC FOCUS (M2000 ONLY)

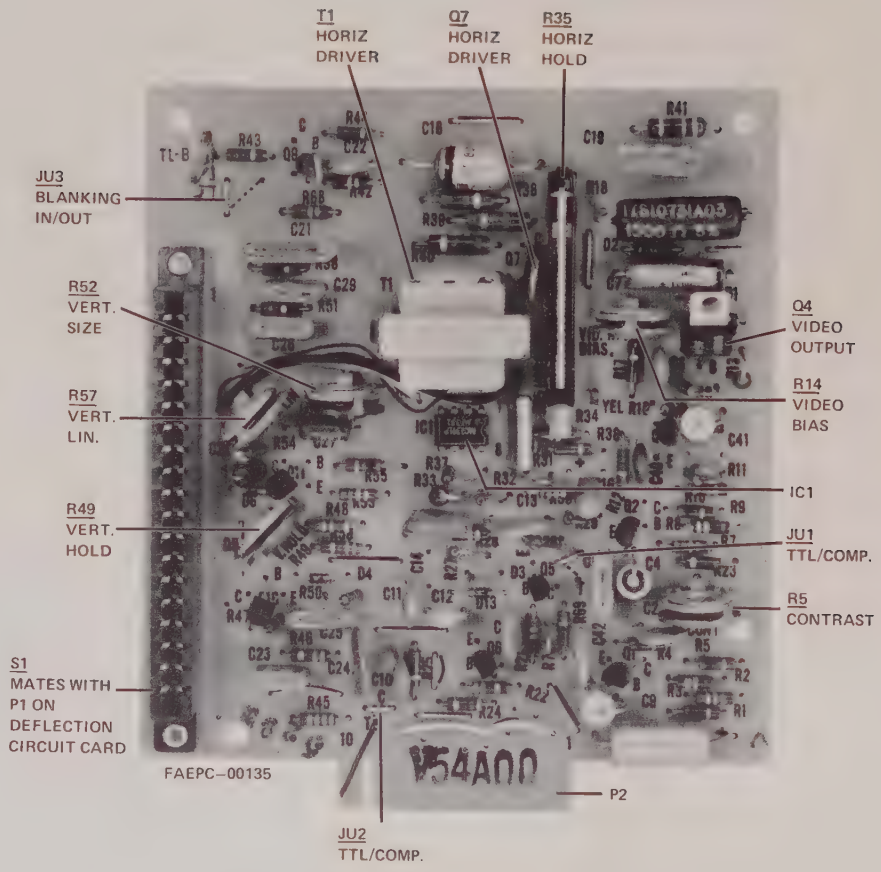
(Reference Figure 6.)

Due to the geometry of a CRT, the electron beam travels a greater distance when deflected to a corner as compared to the distance traveled at the center of the CRT screen. As a result of these various distances traveled, optimum focus can be obtained at only one point. An adequate adjustment can be realized by setting the focus while viewing some point midway between the center of the CRT screen and a corner, thus optimizing the overall screen focus. One of the simplest methods for improvement is to modulate the focus voltage at a horizontal sweep rate. Now optimum focus voltage is made variable on the horizontal axis of the CRT, which compensates for the beam travel along this axis.

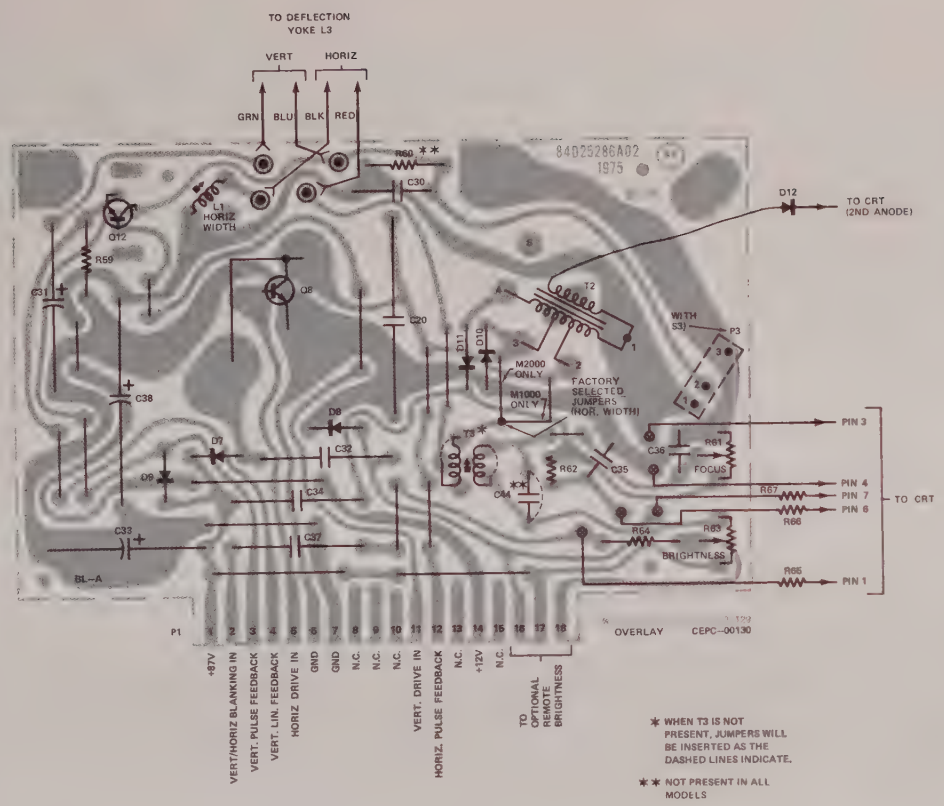
In the M2000, the secondary of T3 generates a parabolic voltage, which together with a fixed voltage from the FOCUS control R61, is applied to the focus grid of V1. This system dynamically changes the value of focus voltage from the CRT screen center to screen edge, which will always provide an optimum amount of voltage for best overall focus.



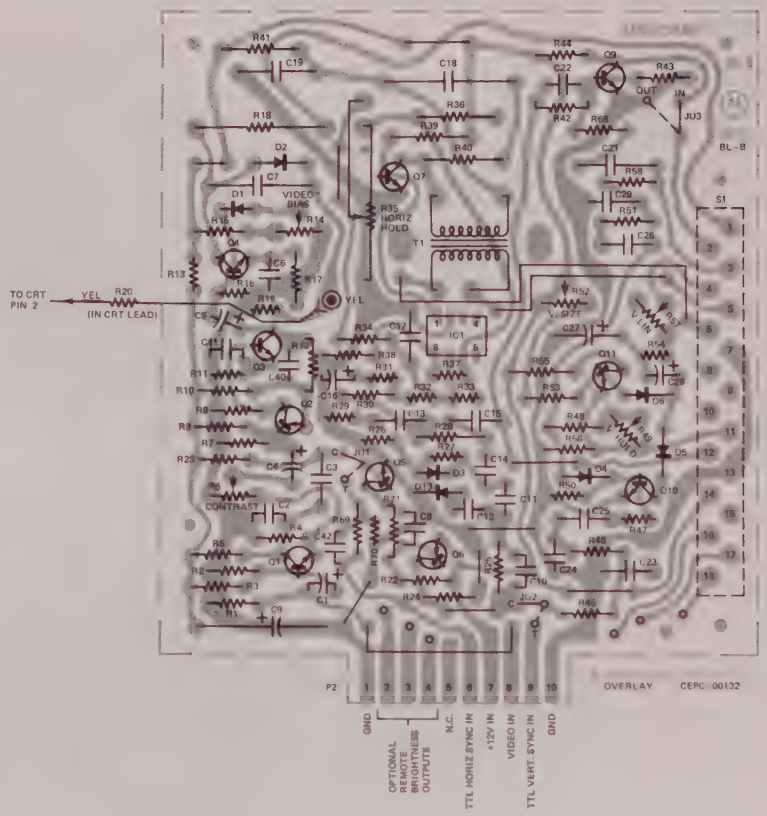

Deflection Circuit Card — Component Side



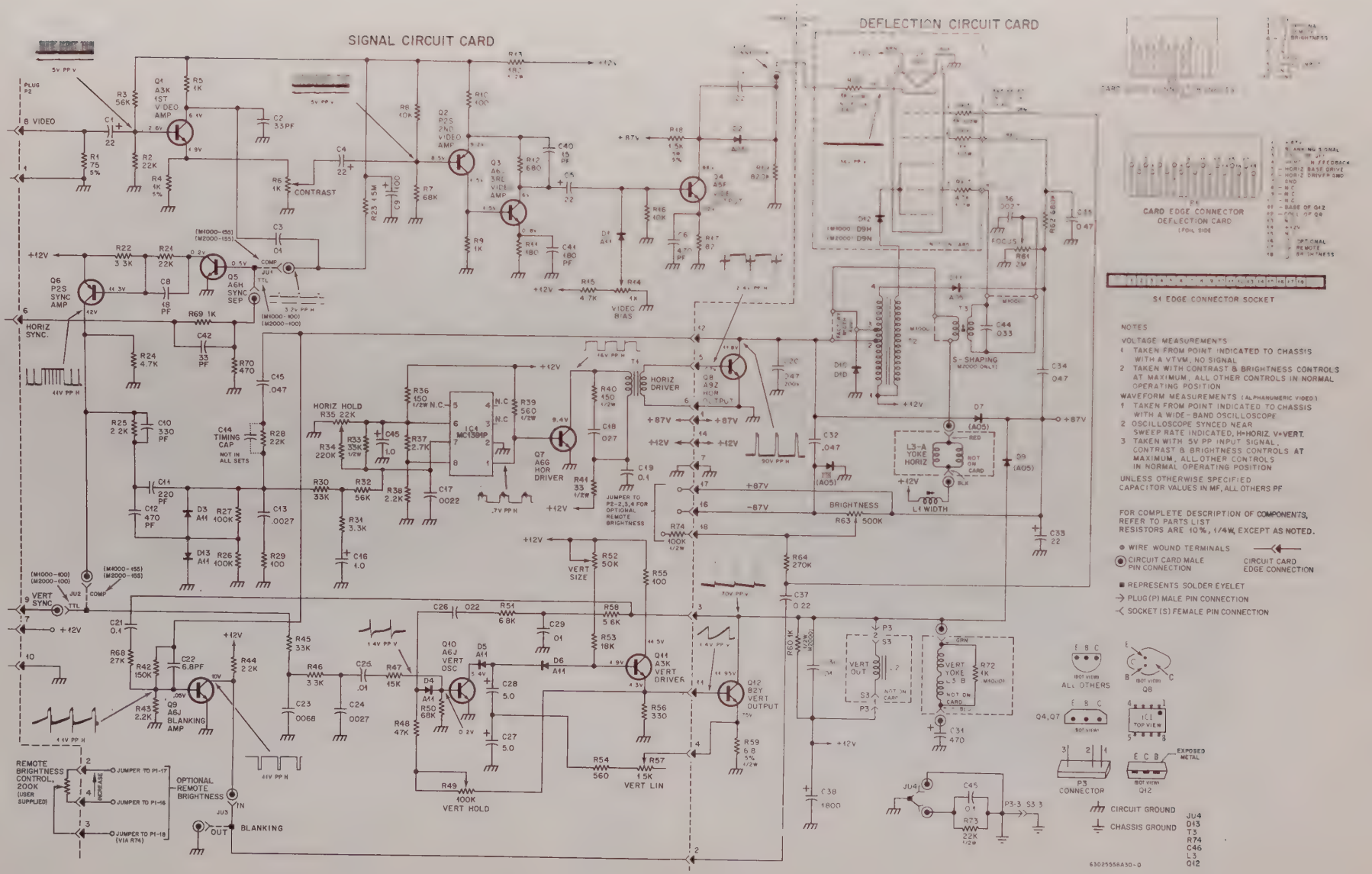

Signal Circuit Card — Component Side



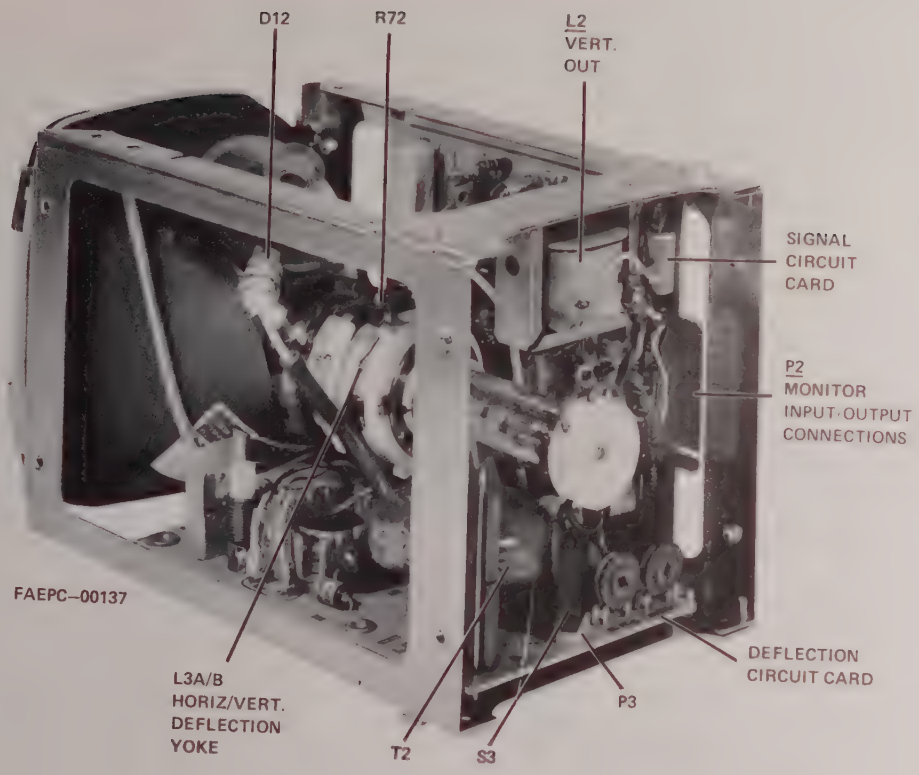

Deflection Circuit Card — Solder Side



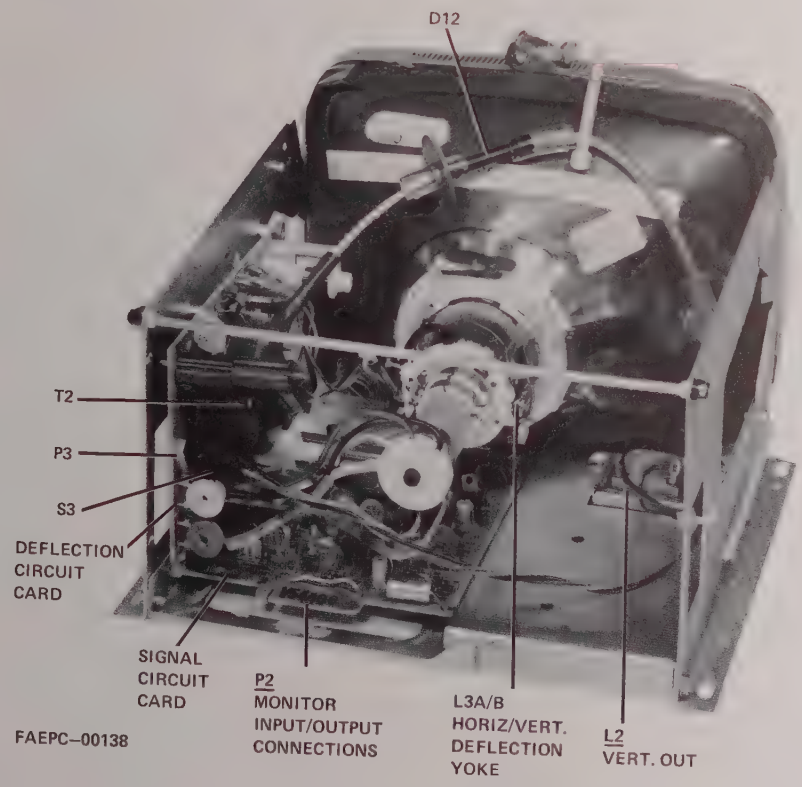

Signal Circuit Card — Solder Side


SIGNAL CIRCUIT CARD
DEFLECTION CIRCUIT CARD
B VIDEO
HORIZ SYNC.
VERT SYNC.
+12V
CONTRAST
HORIZ HOLD
VERT SIZE
VERT HOLD
VERT LIN
BRIGHTNESS
S-SHAPING
L4 WIDTH
BLANKING
REMOTE BRIGHTNESS CONTROL, 200K (USER SUPPLIED)
OPTIONAL REMOTE BRIGHTNESS
CARD EDGE CONNECTOR DEFLECTION CARD
S1 EDGE CONNECTOR SOCKET
NOTES
VOLTAGE MEASUREMENTS
1 TAKEN FROM POINT INDICATED TO CHASSIS WITH A VTVM, NO SIGNAL
2 TAKEN WITH CONTRAST & BRIGHTNESS CONTROLS AT MAXIMUM, ALL OTHER CONTROLS IN NORMAL OPERATING POSITION
WAVEFORM MEASUREMENTS (ALPHANUMERIC VIDEO)
1 TAKEN FROM POINT INDICATED TO CHASSIS WITH A WIDE-BAND OSCILLOSCOPE
2 OSCILLOSCOPE SYNCED NEAR SWEEP RATE INDICATED, H=HORIZ, V=VERT.
3 TAKEN WITH 5V PP INPUT SIGNAL, CONTRAST & BRIGHTNESS CONTROLS AT MAXIMUM, ALL OTHER CONTROLS IN NORMAL OPERATING POSITION
UNLESS OTHERWISE SPECIFIED CAPACITOR VALUES IN MF, ALL OTHERS PF
FOR COMPLETE DESCRIPTION OF COMPONENTS, REFER TO PARTS LIST
RESISTORS ARE 10%, 1/4W, EXCEPT AS NOTED.
WIRE WOUND TERMINALS
CIRCUIT CARD MALE PIN CONNECTION
CIRCUIT CARD EDGE CONNECTION
REPRESENTS SOLDER EYELET
PLUG (P) MALE PIN CONNECTION
SOCKET (S) FEMALE PIN CONNECTION
P3 CONNECTOR
CIRCUIT GROUND
CHASSIS GROUND
JU4 D13 T3 R74 C46 L3 Q12
63025558A30-0

M1000 – 100, 155 and M2000 – 100, 155 – Schematic Diagram




Model M1000 – Rear Chassis View




Model M2000 – Rear Chassis View

# REPLACEMENT PARTS LIST

| REF. NO | PART NUMBER | DESCRIPTION |
|---|---|---|
| | | MONITOR CIRCUIT CARDS (COMPLETE): Order by Model Number and description. |
| **CAPACITORS** (Values are in microfarads unless otherwise noted) | | |
| | 23S187A2[illegible] | 22, 40V; lytic |
| | 21S180C64 | [illegible] pF 10%, N750, 100V; Cer Disc |
| | 8S10191B98 | .01 10%, 250V; Polyester |
| | 23S187A2[illegible] | 22, 40V; lytic |
| | 21S1801[illegible] | 470 pF 10%, X5F; Cer. Disc |
| | 10212A91 | [illegible] 10%, 250V; Mtlz Poly |
| | 21S180[illegible] | 18 pF 5%, NP0; Cer. Disc |
| | 23S10255A0[illegible] | 100, 16V; lytic |
| | 21S1316[illegible] | 330 pF 10%, X5F; Cer. Disc |
| | 21S180B87 | 220 pF 10%, X5F; Cer. Disc |
| | 21S180B53 | 470 pF 10%, X5F; Cer. Disc |
| | 21S180C41 | .0027 10%, Z5F; Cer. Disc |
| | 8S10191B91 | .047 10%, 250V; Polyester |
| | 23S10229A32 | 1.0, 16V; Tant. lytic |
| | 8S10299B24 | .0022 10%, 400V; Poly Carb |
| | 8S10191B88 | .027 10%, 400V; Polyester |
| | 8S10191C02 | 0.1 10%, 250V; Polyester |
| | 8S10072A44 | .047 10%, 200V; Polyester |
| | 8S10191C02 | 0.1 10%, 250V; Polyester |
| | 21S180D93 | 6.8 pF ±0.5 NP0; Cer. Disc |
| | 8S10191B97 | .0068 10%, 400 V; Polyester |
| | 21S180C41 | .0027 10%, Z5F; Cer. Disc |
| | 8S10191B98 | .01 10%, 250V; Polyester |
| | 8S10191B89 | .022 10%, 250V; Polyester |
| [illegible]28 | 23S10218A31 | 5.0, 15V; Tant. lytic |
| C29 | 8S10191B98 | .01 10%, 250V; Polyester |
| C30 | 8S10191A16 | .01 10%, 400V; Polyester |
| C31 | 23S10255A29 | 470, 16V; lytic |
| C32 | 8S10191B07 | .047 10%, 400V; Polyester |
| C33 | 23S10255A74 | 22, 160V; lytic |
| C34 | 8S10191B07 | .047 10%, 400V; Polyester |
| C35 | 8S10212B20 | 0.47 10%, 400V; Mtlz. Poly. |
| C36 | 21S180C41 | .0027 10%, Z5F, 500V; Cer. Disc |
| C37 | 8S10191A53 | 0.22 10%, 160V; Polyester |
| C38 | 23S10255B83 | 1800, 16V; lytic |
| C40 | 21S180C07 | 15 pF 10%, N150; Cer. Disc |
| C41 | 21S180B89 | 180 pF 10%, Z5F 100V; Cer. Disc |
| C42 | 21S180C82 | 33 pF 10%, N150; Cer. Disc |
| C44 | 8S10169B71 | .033 10%, 400V; Mylar (M2000 only) |
| C45 | 23S10229A32 | 1.0, 16V; Lytic |
| C46 | 8S10212D52 | 0.1,100V; Cer. Disc |
| **DIODES** | | |
| D1 | 48D67120A11 | Diode, Low Power; All |
| D2 | 48S191A05 | Rectifier, Silicon; 91A05 |
| D3-D6 | 48D67120A11 | Diode, Low Power; All |
| D7-D9 | 48S191A05 | Rectifier, Silicon; 91A05 |
| D10 | 48S134921 | Diode, D1D |
| D11 | 48S191A05 | Rectifier, Silicon; 91A05 |
| D12 | 48S137608 | Diode, D9H (M1000 only) |
| D12 | 48S137622 | Diode, D9N (M2000 only) |
| D13 | 48D67120A11 | Diode, Low Power; All |
| **INTEGRATED CIRCUIT** | | |
| IC1 | 51S10778A01 | MC1391P; T3L |
| **COILS/CHOKES** | | |
| L1 | 24D25248C07 | Coil, Horiz. Width (M1000 only) |
| L1 | 24D25248C08 | Coil, Horiz. Width (M2000 only) |
| L2 | 25D25221A09 | Choke, Vert. Out |
| L3A/B | 24D25290A02 | Yoke, Deflection (M1000 only) |
| L3A/B | 24D68531A03 | Yoke, Deflection (M2000 only) |

| REF. NO. | PART NUMBER | DESCRIPTION |
|---|---|---|
| **TRANSISTORS** | | |
| Q1 | 48S134997 | 1st Video Ampl.; A3K |
| Q2 | 48S137127 | 2nd Video Ampl.; P2S |
| Q3 | 48S137172 | 3rd Video Ampl.; A6J |
| Q4 | 48S137093 | Video Output; A5F |
| Q5 | 48S137171 | Sync Sep.; A6H |
| Q6 | 48S137127 | Sync Ampl.; P2S |
| Q7 | 48S137169 | Horiz. Driver; A6G |
| Q8 | 48S137462 | Horiz. Output; A9Z |
| Q9 | 48S137172 | Blanking Ampl.; A6J |
| Q10 | 48S137172 | Vert. Osc.; A6J |
| Q11 | 48S134997 | Vert. Driver; A3K |
| Q12 | 48S137598 | Vert. Output; B2Y |
| **RESISTORS/CONTROLS** | | |
| Note: Only power or special resistors are listed. Use the description when ordering standard values of fixed carbon resistors up to 2 watts. | | |
| R6 | 18D25245A02 | Control, Contrast 1k |
| R14 | 18D25245A02 | Control, Video Bias 1k |
| R18 | 17S10731A03 | 1.5k 5%, 5W; Wire Wound |
| R35 | 18C25267B01 | Control, Horiz. Hold 22k |
| R49 | 18D25245A15 | Control, Vert. Hold 100k |
| R52 | 18D25245A20 | Control, Vert. Size 50k |
| R57 | 18D25245A10 | Control, Vert. Lin. 1.5k |
| R61 | 18D25245A12 | Control, Focus 2 Meg. |
| R63 | 18D25245A07 | Control, Brightness 500K |
| **TRANSFORMERS** | | |
| T1 | 25D25221A04 | Transformer, Horiz. Driver |
| T2 | 24D25291C02 | Transformer, High Voltage (M1000 only) |
| T2 | 24D25291C03 | Transformer, High Voltage (M2000 only) |
| T3 | 24D25248A09 | Transformer, S-Shaping (M2000 only) |
| **MISC. ELECTRICAL PARTS** | | |
| V1 | 96S10769A01 | 5"-CRT, Type No. 140ANB4 (M1000 only) |
| V1 | 96S10793A01 | 9"-CRT, Type No. 9VADP4 (M2000 only) |
| **MECHANICAL PARTS** | | |
| | 42D25298A03 | Connector, Anode (M1000 only) |
| | 42D25298A08 | Connector, Anode (M2000 only) |
| S1 | 9S10768A01 | Connector, Receptacle; Header |
| P3 | 28S10586A14 | Connector, Circuit Card; 3-contacts |
| | 26C25198A03 | Heat Sink (for Q8) |
| | 26S10251A08 | Heat Sink (for Q12) |
| S3 | 15S10183A87 | Housing, Receptacle; 3-contact (less contacts) |
| | 39S10184A72 | Contact, Receptacle (3 Req'd for S3) |
| | 14A25340A01 | Insulator, Hi-Voltage Standoff (M2000 only) |
| | 59C25465A02 | Magnet, Focus (M2000 only) |
| | 2S10054A36 | Nut, Clip-on #8-18 (M1000 only) |
| | 42C25258A01 | Retainer, CRT (M1000 only) |
| | 3S138210 | Screw, #8-18 x 1-1/4" (M1000 only) |
| | 26C25323A01 | Shield, Linearity (CRT) |
| | 9D25241A04 | Socket, CRT (Incl. leads and resistors R20, R65, R66 & R67) |
| | 41B25268A03 | Spring, CRT Aquadag (M1000 only) |
| | 41D65987A01 | Spring, Special; CRT Aquadag Gnd (M2000 only) |
| | 42D67027A14 | Strap, CRT Mtg. (M2000 only) |
| | 7S10747A02 | Support Guide, Circuit Card |

POWER-ONE Inc.
531 DAWSON DR.
CAMARILLO, CALIF. 93010
(805) 484-2806

APPLICATION DATA
Including:
1. Schematic
2. Parts Lists
3. Specification
4. Outline & Mounting Dwg.
5. General User Information

MODEL

HCBB-75W

SPECIFICATIONS

AC Input: 115/230 VAC± 10% 47-440 HZ(Derate Current 10% for 50 HZ operation)

Input Fusing: See Table

DC Output: 5VDC at 6A, OVP at 6.2 ±.4VDC
and ±12VDC at 1.7A
or ±15VDC at 1.5A

Line Regulation: ± .05% for a 10% input change

Load Regulation: ± .05% for a 50% load change

Output Ripple: 1.5 mv PK-PK, 0.4 mv RMS

Transient Response: 30μ sec for 50% load change

Overload & Short Circuit Protection: Automatic current limit/foldback

Temperature Coefficient: ± .03%/°C maximum

Cooling: Units are full rated to 50°C in free air, must be derated or fan cooled when mounted in confined area

Temperature Rating: 0 - 50°C, full rated, derate linearly to 40% at 70°C

Efficiency: 55% at nominal input, full load on output

Weight: 8 lbs.

Vibration: Per Mil-Std-810B, method 514, proc. I, curve AB (to 50H7)

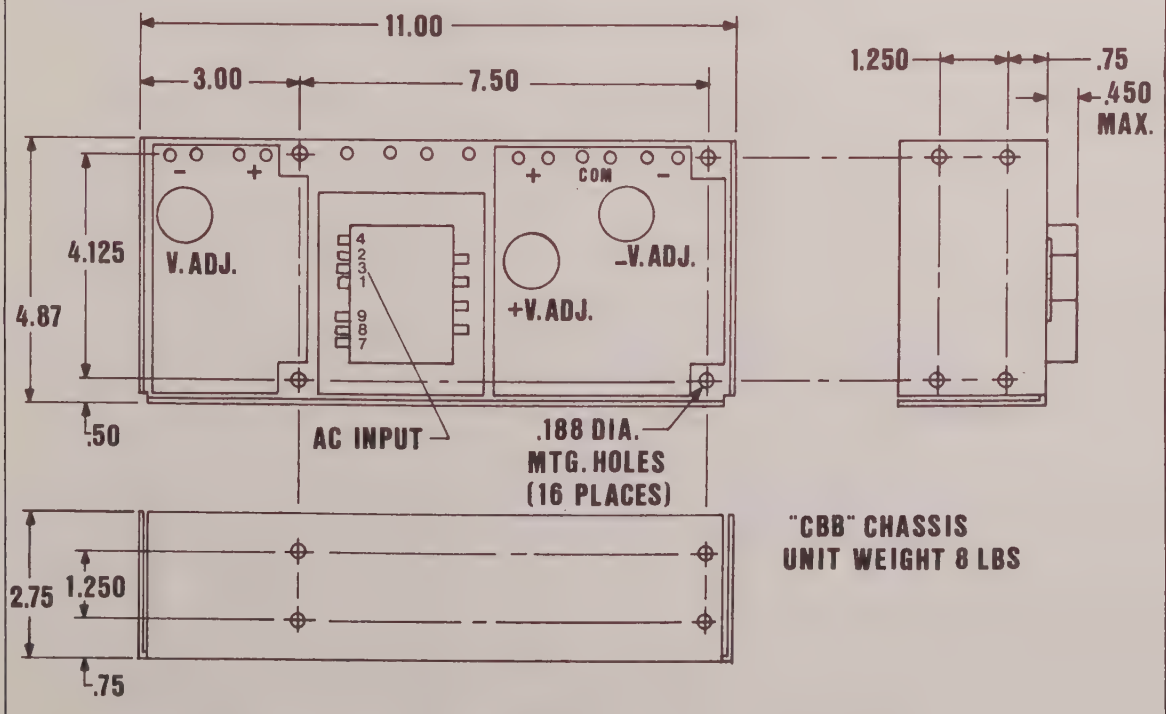
Shock: Per Mil-Std-810B, method 516, procedure V

AC Connection & Fuse Table

| For Use At | Primary Fuse At | Connect | Apply Power to |
|---|---|---|---|
| 115 | 2A | 1-3, 2-4 | 1 & 4 |
| 230 | 1A | 2-3 | 1 & 4 |

2 YEAR GUARANTEE

POWER-ONE will repair or replace any power supply of its manufacture that does not perform to published specifications as a result of defective materials or workmanship for a period of 2 years from date of original purchase. No other obligations or liabilities are implied or expressed. Returns must be freight prepaid.

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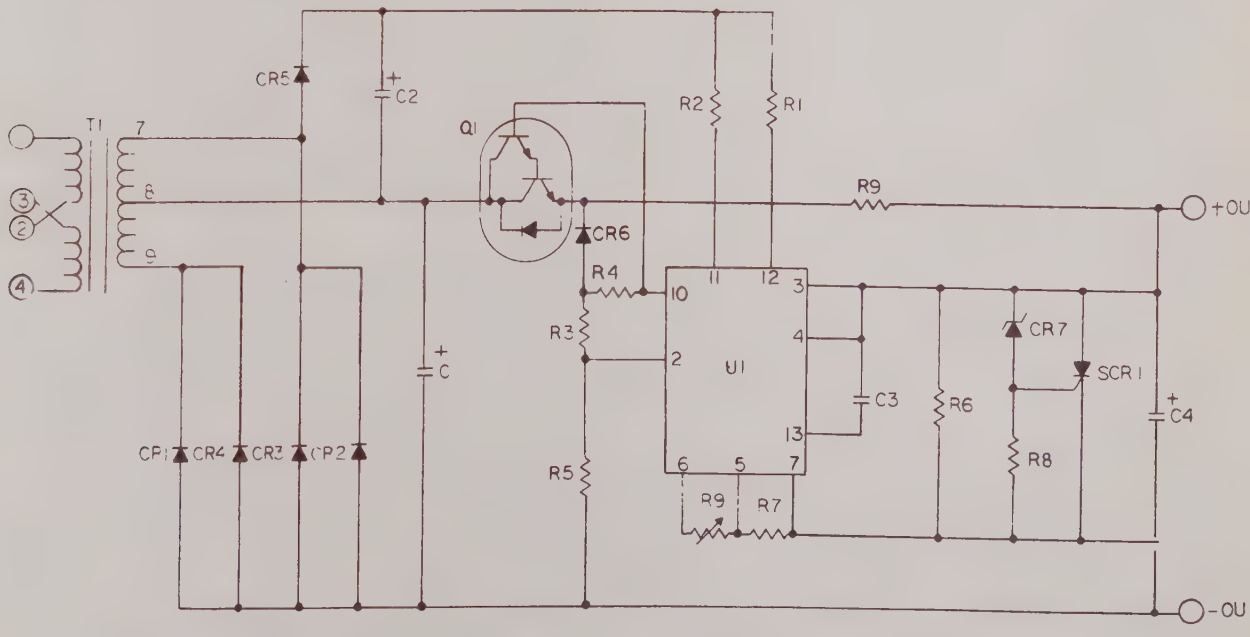
| REF DES | HC5-6 OVP | | DESCRIPTION |
|---|---|---|---|
| C1 | 16000/15 | | CAPACITOR ALUM. ELECT. |
| C2 | 220/16 | | 〃 〃 〃 |
| C4 | 1000/16 | | 〃 ALUM. ELECT. |
| C3 | .01/100 | | CAPACITOR MYLAR |
| | | | |
| | | | |
| CR2,1 | MR750 | | DIODE 6A 50V |
| CR5,6 | AE1C | | 〃 1A 200V |
| CR7 | IN752A | | DIODE ZENER |
| | | | |
| SCR1 | S0508LS3 | | SCR 8A |
| | | | |
| Q1 | 2N6055 | | TRANSISTOR POWER NPN |
| | | | |
| | | | |
| R1,2,3,4,6 | 300Ω | | RESISTOR 1/2W CARBON |
| R7 | 2.2K | | 〃 〃 〃 |
| R5 | 4.7K | | 〃 〃 〃 |
| R8 | 47Ω | | RESISTOR 1/2W CARBON |
| | | | |
| R9 | 1.5K | | POTENTIOMETER |
| | | | |
| | | | |
| U1 | μa723 | | I.C. VOLTAGE REGULATOR |
| | | | |
| T1 | 12247 | | TRANSFORMER |
| | | | |
| PCB | 12098 | | PRINTED CIRCUIT BOARD |
| | | | |
| CHASSIS | 11031 | | CHASSIS ALUM |

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UNAUTHORIZED USE THEREOF IS PROHIBITED

# APPENDIX D

## STATIC HANDLING PRECAUTIONS OF MOS, LSI LOGIC

The 6800 microprocessor, 2708, 2704, 2102, 8080, 8111, 8251, and 8255 are particularly susceptible to static electricity. They can be easily damaged if proper care is not taken in handling them. For this reason, the following steps should be adhered to as closely as possible:

1. All equipment (soldering iron, tweezers, tools, solder, etc.) should be at the same potential as the PC card, the assembler, the work surface, and the IC itself along with black conductive foam. This can be accomplished by continuous physical contact with the work surface, the components, and everything else involved in the operation.

2. When handling the IC, develop the habit of first touching the black conductive foam or conductive container in which it is stored before touching the IC itself. Don't store in other types of foam.

3. Always touch the ground plane of the MPU, SUD, or PM before touching the IC to the board. Try to maintain this contact as much as possible while installing the IC.

4. Handle the IC by the ends. Avoid touching the pins as much as possible.

5. In general, never touch anything to the IC that you have not touched first while touching both it and the IC itself.

6. The end of the personality module 40-pin cable has the same conditions when the microprocessor is in the personality module.

The connector pins of Integrated Circuit chips are very fragile and can be easily pushed out of line. In fact, sometimes IC's will arrive with one or more pins out of line. Trying to install a misaligned IC is a hapless task and, worse, might cause permanent damage to the chip. Lay a small piece of aluminum on the black conductive foam. Lay the IC on its side on the aluminum surface, hold the chip by its ends and exert enough pressure so that all pins are perpendicular to the body.

# APPENDIX E

## MNEMONICS TABLE

ADCOMP = Address Compare - RD to RC
ADTC = Address Terminal Count - RD to RC
APAGE = Able Page RAM - MPU
ARBUF = Address Record Buffer - MPU to RD
ARMA = Auto Arm - FP to RC
ARMM = Manual Arm - FP to RC
ARMED = RC to RD
AROM = Able Read Only Memory - MPU
AROM 1,2,3 = Able ROM - MPU
ASL = Active Scan Line - CRT
BA = Bus Available -MPU to CRT
BCD = Blank Character Display - CRT
Blink = CRT
Blink Bit = MPU to CRT - DB7
BUFF = Buffer Full - RC to FP
CCRT = CRT Clock = 4.4016 MHz MPU
CHCT3 = Character Count 3 - CRT
CLR = Clear - FP to MPU - FP to MPU
COMPV = Composite Video - CRT to Monitor
CPP1 = Clock Pulse Phase 1 - MPU
CPP2 = Clock Pulse Phase 2 - MPU
CCP2D = Delayed CPP2 - RD
CPRC = Clock Pulse Row Counter - CRT
CPVSR = Clock Pulse Video Shift Register - RC to RD
CURSOR BIT = CRT
$\overline{\text{DBE}}$ = Data Bus Enable - CRT
DBE = Data Bus Enable - MPU
DCC = Dot Counter Clock - CRT
DELØ = Delay Out = 0 - RD to RC
DELSTA = Delay Start - FP to RC
DELSTP = Delay Stop - FP to RC
$\overline{\text{DMAR}}$ = Direct Memory Access Request - CRT to MPU
DISSOUT = Delayed Start/Stop Out - RC - FP BNC
EOSTP = End of Storage Stop Event - RC
EXARM = External ARM - FP to RC
EXSTA = External Stop - FP to RC
GO = Go RC
HALT = MPU
HOR SYNC = CRT
LBCP = Line Buffer Clock Pulse - CRT
LO1,2,3,4 = Load Sequence - RC to RD
MASTA = Manual Start - FP to RC
MASTP = Manual Stop - FP to RC
MOABE = Microprocessor Out Address Bus Enable - MPU
MODBE = Microprocessor Out Data Bus Enable - MPU

MPBA = Microprocessor Bus Available - MPU - CRT
MPSTA = Microprocessor Start - DB to RC
MPSTP = Microprocessor Stop - DB to RC
MPIDBE = Microprocessor Input Data Bus Enable - MPU
MPSTAR = Microprocessor Start Record - RC
MPSTPR = Microprocessor Stop Record - RC
MRST = Manual Reset - MPU to RC to CRT
OSCP = Oscillator Clock Phase - MPU 22.008 MHz
NORGO = Normal Go Message - DB to RC
NORSIG = Normal = Hi, Single = Lo - RC
NOSTP = Normal Stop Event - DB to RC
PEVSR = Parallel Entry Video Shift Register - CRT
POR = Preset Out Read - MPU
PRDBE = Page RAM Data Bus Enable - MPU
RAMR = RAM Read - MPU
Read = MPU
RDRB = Read Record Buffer - RD
RDREB = Read Record Bus Buffers - RD
RECAL = Record All - DB to RC
RECBF = Record Buffer - RC to RD
RECDL = Record Latch - RC
RECDM = Record Direct Memory - RC
RECMP = Record Microprocessor to RC
RECRD = Record - RC to MPU to FP
RECW = Record Write - RC to RD
RED A,B = Read A&B - RC to FP
REDl,2,9,8 = Read Delay - FP to RC
RESCONL = Reset Control - RC to RD
R/W = Read/Write - MPU to FP to RD
SCPSYN = Scope Sync - CRT to MPU
STVAD = Set Valid Data - RC
SlGO = Single Go Message - RC
SLl = Scan Line 1 - CRT
SLl0 = Scan Line 10 - CRT
SMDl-9 = Simulated Data - FP
STAEN = Start Enable - RC to RD
STAERW = Start Event Read/Write
STAOT = Start Out Trigger - RC to FP BNC
STARTE = Start Event - RC
STARTL = Start Latch - RC
STASH = Start Search - RC to FP
STAWQ = Start Write Qualifier - DB to RC
STOPEL = Stop Event Latch
STOPE = Stop Event Read/Write - RC
STPOT = Stop Output Trigger - RC to FP
STPSH = Stop Search - RC to FP
STPWQ = Stop Write Qualifier - DB to RC
SUA 0-15 = SUD Address Lines - SUD to PM to RD
SUD 0-7 = SUD Data Lines - SUD to PM to RD
SUD5 = SUD Data Line 5 - SUD to PM to RD
SUDlC = 6800 SUD Personality = High SUD to RD
$\overline{\text{SUDlC}}$ = 8080 SUD Personality = High - SUD to RD
SUDCPl = SUD Clock Phase 1 - SUD to PM to RD to RC
SUDCP2 = SUD Clock Phase 2 - SUD to PM to RD to RC

SUDESI = SUD End Single Instruction - SUD to PM to RD to RC
SUDMAA = SUD Memory Access Acknowledge - PM to RD to RC
SUDMAC = SUD Memory Access Clock - PM to RD to RC
SUDMAR = SUD Memory Access Request - PM to RD to RC
SUDMPE = SUD Microcprocessor Enable - RC to RD to PM to SUD
SUDR = SUD Read - SUD to PM to RD to RC
SUDVMA = SUD Valid Memory Address - SUD to PM to RD to RC
SWSTAT = Switch Status - PM to RD to RC
SYNC = Synchronize - SUD 8080 to PM to RD to RC
VADAT = Valid Data - RC to RD to DB to MPU
Veritical Sync = CRT to Monitor
VIDCO = CRT to Monitor
VMA = Valid Memory Address - MPU to RD
V = Active Video Period - CRT
D = Inactive Video Period - CRT
WCS = Write Chip Select - RD
Write = MPU
Ø1 = CPU Phase 1 Clock - MPU
Ø2 = CPU Phase 2 Clock - MPU

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